VHDL
Initiative
Towards
ASIC
Libraries

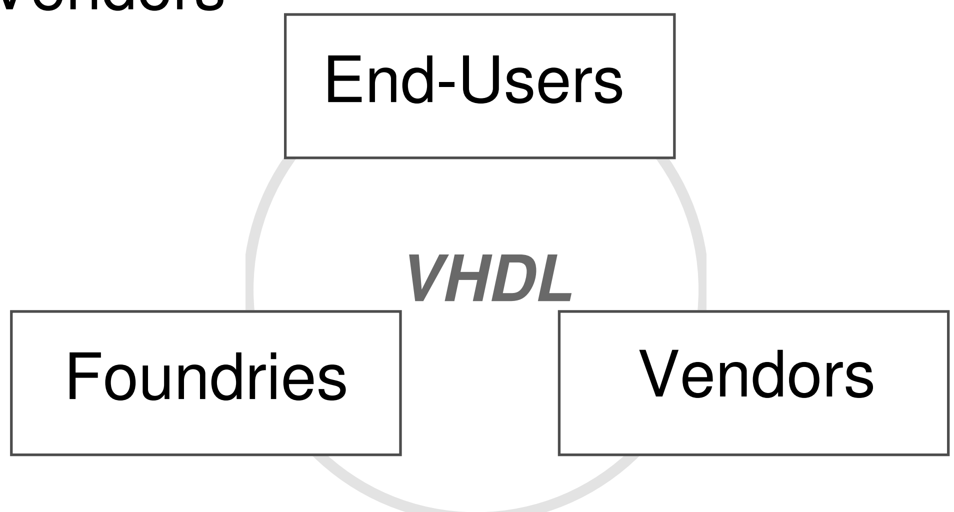
VHDL Initiative Toward ASIC Libraries

What is VITAL?

- Industry-backed initiative inspired by end-users
- Formed to accelerate the availability of ASIC libraries in VHDL
- Leveraging existing standard practices

VITAL Representation Across All Three Groups

- End-Users
- Silicon Foundries
- EDA Vendors



Cadence's Role in VITAL

- Costello provided initial spark for VITAL at VIUF
- Cadence proposed initial strawman leveraging features of Verilog and SDF (Standard Delay Format)
- Organized early supporters and marketing efforts
- Encouraged external coordinator lead following DAC
- Continuing to provide administrative resources
- Technical input (at same level as other participants)

VHDL as a Standard Today

- Driven by IEEE & VHDL International (VI)
- Large Emerging Market
- Recognized worldwide commercial standard
- Simulators are now production worthy
- Single biggest factor limiting rate of adoption:
  Lack of standard modeling practices!

Lack of Standard Modeling Practices

❑ Logic value system	IEEE 1164.1
❑ Resource of pre-defined primitives	?
❑ Standard interchange format for delays	?
❑ Consistent timing models	?
❑ Consistent timing checks	?

Consequence: Proprietary implementations...
Confusion!

User Feedback on VHDL Status

- VHDL design of ASICs needed for top-down, concurrent design processes
- Cannot wait years for definition of modeling practices
- Dissapprove of multiple proprietary implementations
- Need to utilize CAE toolsets more effectively
- Do not want to re-invent a solution for VHDL

Consensus: Need effective solution in VHDL now!

VITAL's Charter

Promote the acceptance of VHDL for ASIC design through the timely availability of ASIC libraries which can be used across industry simulators.

VITAL Approach

- Coordinate inputs from VITAL participants to develop a technical proposal defining specific standard modeling practices, leveraging Verilog, SDF where possible
- Define necessary primitive set, timing models, and style guide to permit rapid availability of existing ASIC libraries
- Work within scope of existing VHDL language definition
- Forward completed proposal to appropriate VHDL standardization groups by 4Q92 for approval

Software-based standardization permits evolutionary path with no required changes to tools!

Technical Details

- Primitive set and timing checks to be provided through definition of VHDL package and package body
- std_logic_1164 will be used; X01Z subtypes can support acceleration, synthesis
- Existing foundry tools for delay calculation may store results in SDF for simulator access during elaboration
- SDF format accessible for other tools in process flow (static timing, synthesis, etc.)

Technical Details: Timing Support

- Support will be provided for the following delay types:
  - module path, device, interconnect, and port

- Delays may be:
  - incremental or absolute
  - conditional or unconditional
  - instance-specific or by type/library

- Timing checks: setup, hold, recovery, skew, width, and period

- Support for scaling, environmental, technology, and user-defined parameters

VITAL
Gained Quick Support

Alcatel NV
Bell Northern Research
Cadence
CLSI Solutions
Dazix/Intergraph
Epson
Ericsson Telecom AB
Expertest
Harris Semiconductor
Magnati Marelli Electronics
Mahtra MHS SA
Motorola
National Semiconductor
NEC Electronics
Nextwave Design Automation
North Oaks EDA Consulting
Oki Semiconductor
Racal-Redac
SMOS/Seiko
SGS Thomson
SimQuest
Sunrise Test Systems, Inc.
Texas Instruments
Thomson CSF
Toshiba
Vantage Analysis Systems
VHDL Technology Group
Xilinx

... and the momentum continues to grow!

Near-Term Plans for VITAL

- Review draft spec; complete requirements document
- Develop timing interface design and naming
- Define primitive set with support of foundries
- Define hooks between timing format and VHDL
- Develop prototype sample libraries with foundries
- Run pilot programs with selected foundries and compare results to verify process
- Deliver ASIC model guide; submit technical proposal

Benefits of VITAL

- For ASIC designers
  - Improved ability to migrate designs
  - Wider selection of ASIC libraries
- For Silicon Manufacturers
  - Single library that supports multiple simulators
  - Reduced development and maintenance costs
- For EDA Vendors
  - Focus on tool and design issues, not libraries
  - Standard modeling techniques allow improved optimization and reduced complexity

Current Organization

- William Billowitch, Technical Coordinator
  VHDL Technology Group, (215) 266-9791
  uunet!vhdl!wdb

- Steven Schulz, North American Coordinator
  Texas Instruments, (214) 575-2720
  ses@asd470.dseg.ti.com

- Erik Huyskens, European Coordinator
  Alcatel NV, 323 240 7535

How to Participate

- ❑ Contact local coordinator or Cadence contact for copies of current VITAL documents
- ❑ Indicate level of interest: work in definition, pilot program, review specs, etc.
- ❑ Get on mailing list for status updates
- ❑ General interest email address: vital-info@clsi.com
- ❑ Encourage ASIC vendors to participate
- ❑ Make suggestions to VITAL on how to improve program