15 Stop-Watch

It has been pointed out by Mike Fourman that this example illustrates the need for temporal abstraction which might be treated differently than the data abstraction found in the arithmetic examples like the *N*-bit adder (section 9) [Four90].

15.1 Specification

Consider designing a digital stopwatch with a three digit, seven-segment display (to read tens of seconds, seconds and tenths of seconds), and two control buttons, "*reset*" and "*start/stop*". When the *reset* button is pressed the display is cleared. The *start/stop* button is used to start and stop the clock. The design is driven by an 1MHz external clock signal. The stop watch is constructed as a synchronous design with one iteration in each clock cycle.

15.2 Implementation

The stopwatch basically consists of 3 synchronous, self starting counters (Fig. 15-1) which generate output data tenths_out, seconds_out, tens_out. For counting the tens of seconds, o modulo 6 counter is used, for counting seconds and tenths of seconds, modulo 10 counters are required. (Fig. 15-2, Fig. 15-3).

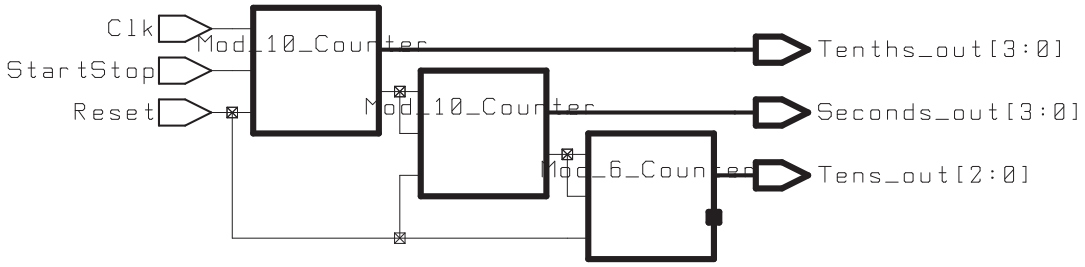

Figure 15-1: StopWatchCount

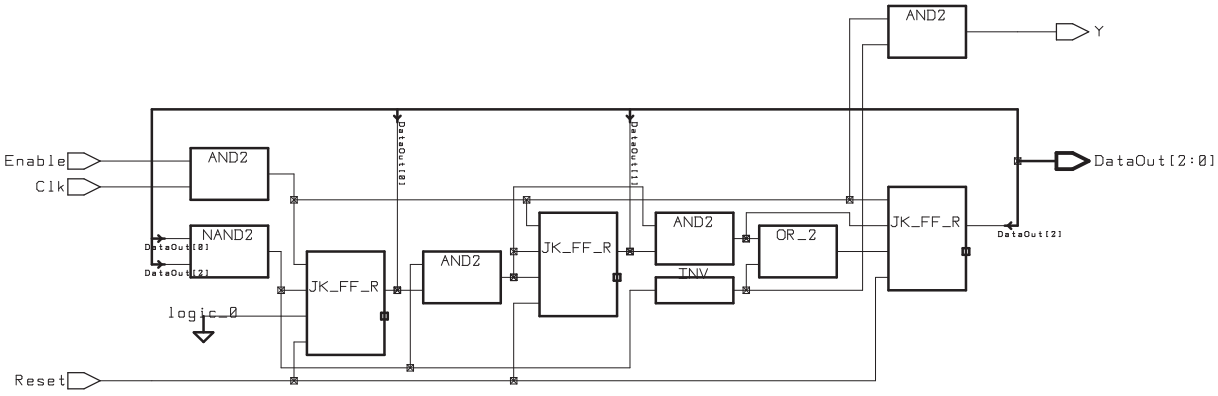

Figure 15-2: Mod_6_Counter

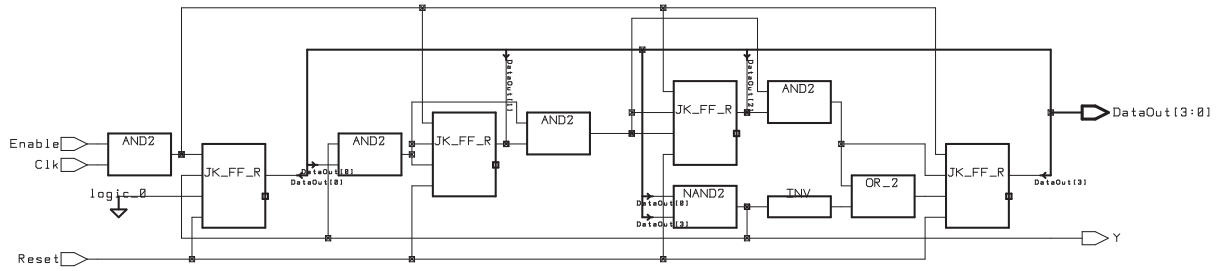

Figure 15-3: Mod_10_Counter

Because of the 1 Mhz clock input, there must be a clock reducing device, build of modulo 10 counters, to generate an internal clock signal (Fig. 15-4).

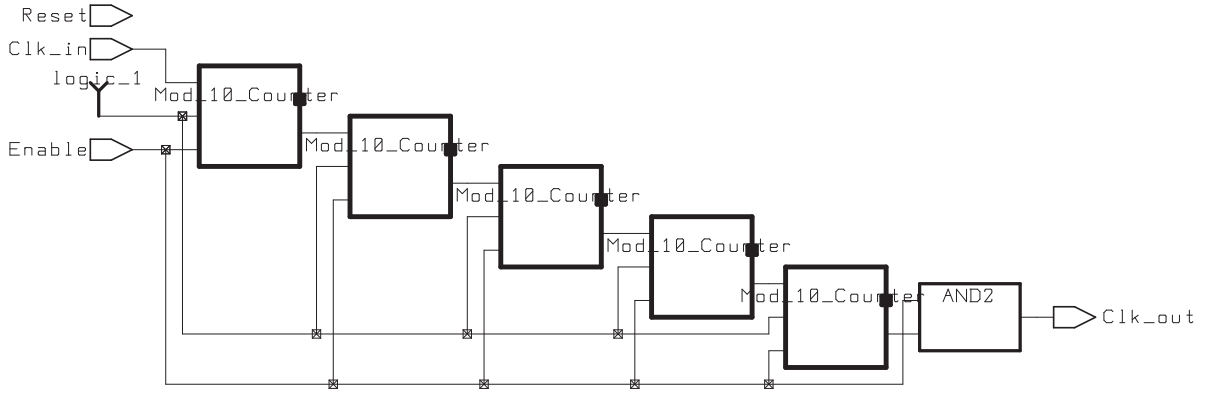

Figure 15-4: StopWatchReduce

In accordance to the specification, a combinational logic is provided to generate the output signals for a 7 segment display out of the data vectors (Fig. 15-5). The overall structure is shown in Fig. 15-6. Fig. 15-7 shows the waveform of the counting device in comparison with a behavioral description of the stopwatch.

15.3 Status and Acknowledgments

The circuit has been originally proposed by J. Staunstrup. Most of the actual text is directly quoted from [Stau93]. Thanks to C.-J. Thomas for generating the VHDL descriptions.

15.4 Literature

[Stau93] J. Staunstrup. IFIP WG 10.2 collection of circuit verification examples, November 1993.

[Four90] M. Fourman. Formal system design. In J. Staunstrup, editor, *Formal Methods for VLSI Design*, pages 191–236. North-Holland/Elsevier, 1990.

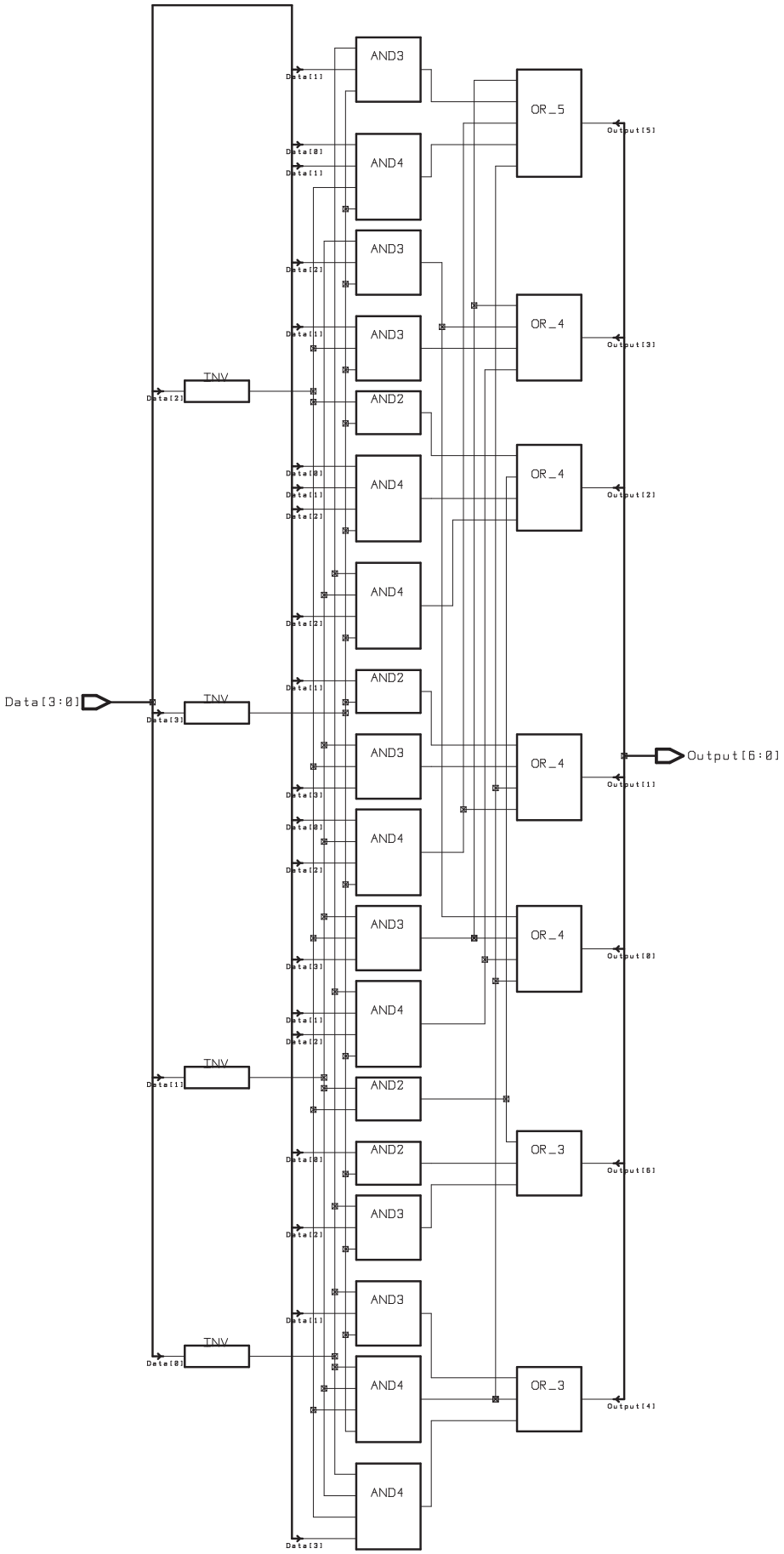

Figure 15-5: Unit for 7 Segment Display

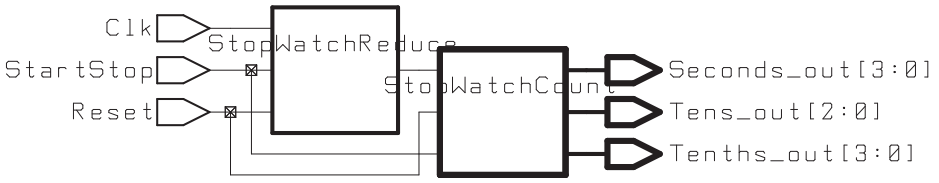

Figure 15-6: Overall Structure of Stop Watch

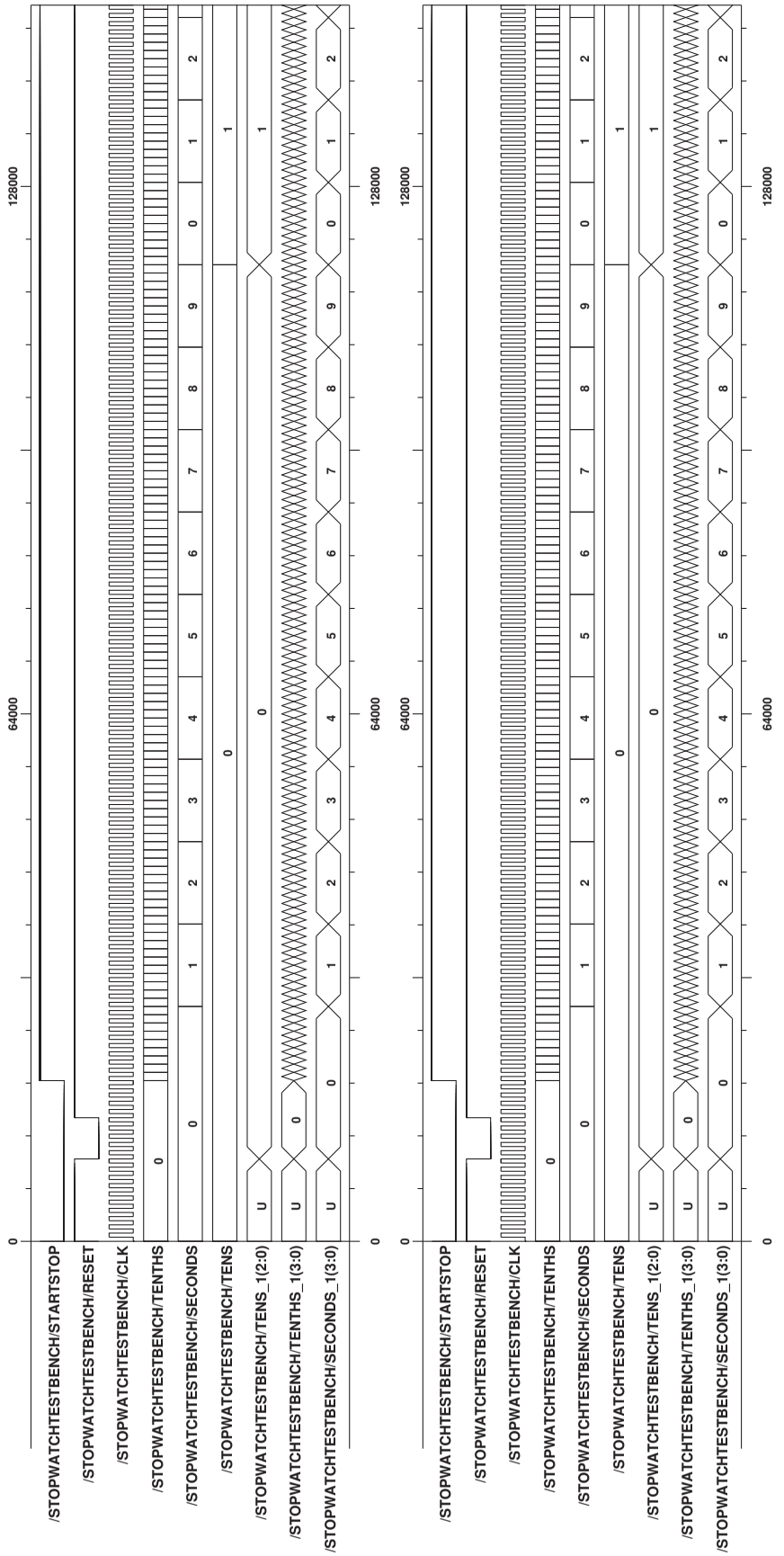

Figure 15-7: Example Waveforms