Stratix Series

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Stratix V FPGA Features

The following features, packages, and I/O matrices give you an overview of our devices. To get the full story, check out our online selector guide. www.altera.com/selector

		Stratix V GT, GX, GS, and E FPGAs (0.85 V), Up to 28G Transceivers[1]					
		5SGTB5	5SGTB7	5SGXA3	5SGXA4	5SGXA5	5SGXA7
Density and Speed	ALMs	160,000	235,000	76,000	113,000	160,000	235,000
	Equivalent LEs	425,000	622,000	200,000	300,000	425,000	622,000
	Registers[2]	642,000	939,000	302,000	452,000	642,000	939,000
	M20K memory blocks	2,304	2,560	1,034	1,316	2,304	2,560
	MLAB memory (Kb)	4,900	7,200	2,300	3,500	4,900	7,200
	Embedded memory (Kb)	45,000	50,000	20,100	25,700	45,000	50,000
	18-bit x 18-bit multipliers	512	512	376	376	512	512
	Speed grades (fastest to slowest)	-2, -3, -4					
Architectural Features	Global clock networks	16					
	Regional clock networks	92					
	Design security	✓					
	HardCopy series device support	✓					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]					
	I/O standards supported	LVTTL, LVCMOS, PCI™, PCI-X™, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)					
	LVDS channels, 1.4 gigabits per second (Gbps) (receive/transmit)	149	149	156	156	210	210
	Embedded dynamic phase alignment (DPA) circuitry	✓					
	Series and differential OCT	✓					
	Transceiver (SERDES) channels (28 Gbps/12.5 Gbps)	4/32	4/32	0/24, 36	0/24, 36	0/24, 36, 48	0/24, 36, 48
	PCIe hard IP blocks	1	1	1, 2	1, 2	1, 4	1, 4
	100G Ethernet hard IP blocks	Yes					
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] All data is preliminary.
[2] 3.3 V compliant, requires a 3-V power supply.

		Stratix V GT, GX, GS, and E FPGAs (0.85 V), Up to 28G Transceivers[1]					
		5SGXB5	5SGXB6	5SGSB7	5SGSB8	5SEB9	5SEBA
Density and Speed	ALMs	152,000	202,000	213,000	267,000	365,000	410,000
	Equivalent LEs	404,000	534,000	563,000	706,000	968,000	1,087,000
	Registers[2]	610,000	806,000	850,000	1,066,000	1,461,000	1,640,000
	M20K memory blocks	1,836	1,989	1,620	1,755	1,596	2,100
	MLAB memory (Kb)	4,700	6,100	6,500	8,100	11,300	12,500
	Embedded memory (Kb)	35,800	38,800	31,600	34,200	33,000	43,000
	18-bit x 18-bit multipliers	612	612	3,240	3,510	1,064	1,100
	Speed grades (fastest to slowest)	-2, -3, -4					
Architectural Features	Global clock networks	16					
	Regional clock networks	92					
	Design security	✓					
	HardCopy series device support	✓					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)					
	LVDS channels, 1.4 Gbps (receive/transmit)	162	162	258	258	225	225
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
	Transceiver (SERDES) channels (28 Gbps/12.5 Gbps)	0/66	0/66	0/27	0/27	0/0	0/0
	PCIe hard IP blocks	1, 4	1, 4	1, 2	1, 2	0	0
	100G Ethernet hard IP blocks	Yes	Yes	Yes	Yes	0	0
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] All data is preliminary.
[2] 3.3 V compliant, requires a 3-V power supply.

Stratix® Series

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Stratix IV GT FPGA Features

		Stratix IV GT FPGAs (0.95 V), 11.3-Gbps Transceivers[1]					
		EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3	EP4S100G4	EP4S100G5
Density and Speed	ALMs	91,200	212,480	91,200	116,480	141,440	212,480
	Equivalent LEs	228,000	531,200	228,000	291,200	353,600	531,200
	Registers[2]	182,400	424,960	182,400	232,960	282,880	424,960
	M9K memory blocks	1,235	1,280	1,235	936	1,248	1,280
	M144K memory blocks	22	64	22	36	48	64
	MLAB memory (Kb)	2,850	6,640	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	14,283	20,736	14,283	13,608	18,144	20,736
	18-bit x 18-bit multipliers	1,288	1,024	1,288	832	1,024	1,024
	Speed grades (fastest to slowest)	-1, -2, -3					
Architectural Features	Global clock networks	16					
	Regional clock networks	64	88	64	88	88	88
	Periphery clock networks	88	112	88	112	112	112
	PLLs/unique outputs	8/68	8/68	8/68	12/96	12/96	12/96
	Design security	✓					
	HardCopy series device support	–					
	Configuration file size (Mb)	95	172	95	172	172	172
	Others	Plug & Play Signal Integriy, Programmable Power Technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)					
	Emulated LVDS channels, 1,100 Mbps	192	256	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	46/46					
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
	Transceiver (SERDES) channels[4] (11.3 Gbps/8.5 Gbps/6.5 Gbps)	12/12/12	12/12/12	24/0/12	24/8/16	24/8/16	32/0/16
	PCIe hard IP blocks	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] Available in industrial temperatures only (0°C to 100°C).
[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.
[3] 3.3 V compliant, requires a 3-V power supply.
[4] The total transceiver count is the sum of 11.3-Gbps plus 8.5-Gbps plus 6.5-Gbps transceivers.

Stratix IV GX FPGA Features

		Stratix IV GX FPGAs (0.9 V), 8.5-Gbps Transceivers[1]						
		EP4SGX70	EP4SGX110	EP4SGX180	EP4SGX230	EP4SGX290	EP4SGX360	EP4SGX530
Density and Speed	ALMs	29,040	42,240	70,300	91,200	116,480	141,440	212,480
	Equivalent LEs	72,600	105,600	175,750	228,000	291,200	353,600	531,200
	Registers[2]	58,080	84,480	140,600	182,400	232,960	282,880	424,960
	M9K memory blocks	462	660	950	1,235	936	1,248	1,280
	M144K memory blocks	16	16	20	22	36	48	64
	MLAB memory (Kb)[2]	908	1,320	2,197	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	6,462	8,244	11,430	14,283	13,608	18,144	20,736
	18-bit x 18-bit multipliers	384	512	920	1,288	832	1,040[3]	1,024
	Speed grades (fastest to slowest)	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -3, -4
Architectural Features	Global clock networks	16						
	Regional clock networks	64	64	64	64	88	88	88
	Periphery clock networks	56	56	88	88	88	88	112
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96	12/96
	Design security	✓						
	HardCopy series device support	✓[5]	✓[5]	✓	✓	✓	✓	✓
	Configuration file size (Mb)	53	53	95	95	141	141	172
	Others	Plug & Play Signal Integrity, Programmable Power Technology						
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[6]						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)						
	Emulated LVDS channels 1,100 Mbps	128	128	192	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	98/98	98/98	98/98
	Embedded DPA circuitry	✓						
	Series and differential OCT	✓						
	Transceiver (SERDES) channels (8.5 Gbps/6.5 Gbps)[7]	16/8	16/8	24/12	24/12	32/16	32/16	32/16
	PCIe hard IP blocks	2	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR						

[1] Maximum LVDS channels, transceiver channels, PLLs/unique outputs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety of options to meet your design needs.
[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.
[3] EP4SGX360N has 1,024 18x18 multipliers.
[4] Support for -2 core and -3 I/O speed-grade. Support for PCIe Gen1 and Gen2 x8. Selected devices only.
[5] For EP4SGX70D and EP4SGX110D/F devices.
[6] 3.3 V compliant, requires a 3-V power supply.
[7] The total transceiver count is the sum of 8.5-Gbps transceivers plus 6.5-Gbps transceivers.

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Stratix IV E FPGA Features

		Stratix IV E FPGAs (0.9 V)			
		EP4SE230	EP4SE360	EP4SE530	EP4SE820
Density and Speed	ALMs	91,200	141,440	212,480	325,220
	Equivalent LEs	228,000	353,600	531,200	813,050
	Registers[1]	182,400	282,880	424,960	650,440
	M9K memory blocks	1,235	1,248	1,280	1,610
	M144K memory blocks	22	48	64	60
	MLAB memory (Kb)	2,850	4,420	6,640	10,163
	Embedded memory (Kb)	14,283	18,144	20,736	23,130
	18-bit x 18-bit multipliers	1,288	1,040	1,024	960
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-2, -3, -4	-3, -4
Architectural Features	Global clock networks	16			
	Regional clock networks	64	88	88	88
	Periphery clock networks	88	88	112	132
	PLLs/unique outputs	4/34	12/96	12/96	12
	Design security	✓			
	Configuration file size (Mb)	95	141	172	230
	HardCopy series device support	✓			
	Others	Programmable Power Technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)			
	Emulated LVDS channels, 1,100 Mbps	128	256	256	288
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	112/112	132/132
	Embedded DPA circuitry	✓			
	Series and differential OCT	✓			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR			

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which can increase the total register count by an additional 50 percent.
[2] 3.3 V compliant, requires a 3-V power supply.

Stratix III L FPGA Features

		Stratix III L FPGAs (1.1 V, 0.9 V)					
		EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340
Density and Speed	ALMs	19,000	27,000	42,600	56,800	79,560	135,200
	Equivalent LEs	47,500	67,500	107,500	142,500	198,900	338,000
	Registers[1]	38,000	54,000	85,200	113,600	159,120	270,400
	M9K memory blocks	108	150	275	355	468	1,040
	M144K memory blocks	6	6	12	16	36	48
	MLAB memory (Kb)[2]	297	422	672	891	1,250	2,110
	Embedded memory (Kb)	1,836	2,214	4,203	5,499	9,396	16,272
	18-bit x 18-bit multipliers	216	288	288	384	576	576
	Speed grades (fastest to slowest)	-2, -3, -4					
Architectural Features	Global clock networks	16					
	Regional clock networks	48	48	48	48	88	88
	Periphery clock networks	104	104	208	208	208	208
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96
	Design security	✓					
	Configuration file size (Mb)	22	22	47	47	66	120
	HardCopy series device support	✓					
	Others	Programmable Power Technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	Emulated LVDS channels, 1,100 Mbps	56	56	88	88	112	137
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.
[2] The size of the MLAB ROM is twice the size of the MLAB RAM.

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Stratix III E FPGA Features

		Stratix III E FPGAs (1.1 V)			
		EP3SE50	EP3SE80	EP3SE110	EP3SE260
Density and Speed	ALMs	19,000	32,000	42,600	101,760
	Equivalent LEs	47,500	80,000	107,500	254,400
	Registers[1]	38,000	64,000	85,200	203,520
	M9K memory blocks	400	495	639	864
	M144K memory blocks	12	12	16	48
	MLAB memory (Kb)[2]	297	500	672	1,594
	Embedded memory (Kb)	5,328	6,183	8,055	14,688
	18-bit x 18-bit multipliers	384	672	896	768
	Speed grades (fastest to slowest)	-2, -3, -4			
Architectural Features	Global clock networks	16			
	Regional clock networks	48	48	48	88
	Periphery clock networks	104	208	208	208
	PLLs/unique outputs	4/34	8/68	8/68	12/96
	Design security	✓			
	Configuration file size (Mb)	26	48	48	93
	HardCopy series device support	✓			
	Others	Programmable Power Technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	Emulated LVDS channels, 1,100 Mbps	56	88	88	112
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	88/88	112/112
	Embedded DPA circuitry	✓			
	Series and differential OCT	✓			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR			

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.
[2] The size of the MLAB ROM is twice the size of the MLAB RAM.

Stratix II GX FPGA Features

		Stratix II GX FPGAs (1.2 V), 6.375-Gbps Transceivers[1]			
		EP2SGX30	EP2SGX60	EP2SGX90	EP2SGX130
Density and Speed	ALMs	13,552	24,176	36,384	53,016
	Equivalent LEs	33,880	60,440	90,960	132,540
	Registers[2]	27,104	48,352	72,708	106,032
	M512 memory blocks	202	329	488	699
	M4K memory blocks	144	255	408	609
	M512K memory blocks	1	2	4	6
	Embedded memory (Kb)	1,338	2,485	4,415	6,590
	18-bit x 18-bit multipliers	64	144	192	252
	Speed grades (fastest to slowest)	-3, -4, -5			
Architectural Features	Global clock networks	48			
	Regional clock networks	48			
	PLLs/unique outputs	4/18	8/36	8/36	8/36
	Design security	3			
	Configuration file size (Mb)	10	17	28	40
	HardCopy series device support	–	–	–	–
	Others	Plug & Play Signal Integrity			
I/O Features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, HyperTransport™, Differential SSTL-18, Differential SSTL-2,Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	Emulated LVDS channels, 1,100 Mbps	31/29	42/42	59/59	73/71
	LVDS channels, 1,000 Mbps (receive/transmit)	31/29	42/42	59/59	73/71
	Embedded DPA circuitry	✓			
	Series and differential OCT	✓			
	Transceiver (SERDES) channels (6.375 Gbps)	8	12	16	20
	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR			

[1] Maximum PLLs/unique outputs, LVDS channels, and transceiver channels for the product line shown. Various packages offer a variety of options to meet your design needs.
[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.

Stratix Series

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Stratix Series Package and I/O Matrices

	Stratix V GX and GS FPGAs (0.85 V), Up to 12.5-Gbps Transceivers					
	FineLine BGA (FBGA) (F)					Hybrid FPGA (H)
	1,152 pin 35 x 35 (mm) 1.0 mm pitch	1,152 pin 35 x 35 (mm) 1.0 mm pitch	1,517 pin 40 x 40 (mm) 1.0 mm pitch	1,517 pin 40 x 40 (mm) 1.0 mm pitch	1,932 pin 45 x 45 (mm) 1.0 mm pitch	780 pin 29 x 29 (mm) 1.0 mm pitch
5SGXA3	552, 138, 24	444, 111, 36	624, 156, 36			364, 66, 24
5SGXA4	560, 138, 24	444, 111, 36	624, 156, 36			364, 66, 24
5SGXA5	560, 138, 24	444, 111, 36	696, 174, 36	600, 150, 48	840, 210, 48	
5SGXA7	560, 138, 24	444, 111, 36	696, 174, 36	600, 150, 48	840, 210, 48	
5SGXB5			432, 108, 66		648, 162, 66	
5SGXB6			432, 108, 66		648, 162, 66	
5SGXB7	528, 132, 27		780, 195, 27		1,032, 258, 27	
5SGXB8	528, 132, 27		780, 195, 27		1,032, 258, 27	

288 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and restriction of hazardous substances (RoHS)-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚ to 100˚).

	Stratix IV GX FPGAs (0.9 V), 8.5-Gbps Transceivers[1]					
	FBGA (F)					
	780 pin 29 x 29 (mm) 1.0 mm pitch	1,152 pin 35 x 35 (mm) 1.0 mm pitch	1,152 pin 35 x 35 (mm) 1.0 mm pitch	1,517 pin 40 x 40 (mm) 1.0 mm pitch	1,760 pin 42.5 x 42 (mm) 1.0 mm pitch	1,932 pin 45 x 45 (mm) 1.0 mm pitch
EP4SGX70	368 8+0		480 16+8			
EP4SGX110	368 8+0	368 16+0	480 16+8			
EP4SGX180	368 8+0	560 16+0	560 16+8	736 24+12		
EP4SGX230	368 8+0	560 16+0	560 16+8	736 24+12		
EP4SGX290	288[2] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
EP4SGX360	288[2] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
EP4SGX530			560[3] 16+8	736[3] 24+12	864 24+12	904 32+16

[1] I/O counts do not include dedicated clock inputs that can be used as data inputs.
[2] Hybrid package (flip chip) FBGA: 35.00 x 35.00 (mm) 1.00 mm pitch.
[3] Hybrid package (flip chip) FBGA: 42.50 x 42.50 (mm) 1.00 mm pitch.

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8+0 Values on top indicate available user I/O pins; values at the bottom indicate the 8.5-Gbps plus 6.5-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.
Stratix IV GT devices are only offered in industrial temperatures (0˚C to 100˚C).

	Stratix IV GT FPGAs (0.95 V), 11.3-Gbps Transceivers	
	FBGA (F)[1]	
	1,517 pin 40 x 40 (mm) 1.0 mm pitch	1,932 pin 45 x 45 (mm) 1.0 mm pitch
EP4S40G2	646 12+12+12	
EP4S40G5	646[2] 12+12+12	
EP4S100G2	646 24+0+12	
EP4S100G3		769 24+8+16
EP4S100G4		769 24+8+16
EP4S100G5	646[2] 24+0+12	769 32+0+16

[1] FineLine ball grid array
[2] Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0 mm pitch.

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12+12+12 Values on top indicate available user I/O pins; values on bottom indicate the 11.3-Gbps plus 8.5-Gbps plus 6.5-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚C to 100˚C).

		FBGA (F)				
		484 pin 23 x 23 (mm) 1.0 mm pitch	780pin 29 x 29 (mm) 1.0 mm pitch	1,152 pin 35 x 35 (mm) 1.0 mm pitch	1,517 pin 40 x 40 (mm) 1.0 mm pitch	1,760 pin 42.5 x 42.5 (mm) 1.0 mm pitch
Stratix IV E FPGAs	EP4SE820			736[3]	960[3]	1,104
	EP4SE530			736[3]	960[3]	960
	EP4SE360		480[2]	736		
	EP4SE230		480			
Stratix III E FPGAs[1]	EP3SE260[3]		480[2]	736	960	
	EP3SE110		480	736		
	EP3SE80		480	736		
	EP3SE50	288	480			
Stratix III L FPGAs[1]	EP3SL340			736[3]	960	1,104
	EP3SL200		480[2]	736	960	
	EP3SL150		480	736		
	EP3SL110		480	736		
	EP3SL70	288	480			
	EP3SL50	288	480			

[1] I/O counts do not include dedicated clock inputs that can be used as data inputs.
[2] Hybrid package (flip chip) FBGA: 35.00 x 35.00 (mm) 1.0 mm pitch.
[3] Hybrid package (flip chip) FBGA: 42.50 x 42.50 (mm) 1.0 mm pitch.

288 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚ to 100˚).

	Stratix II GX FPGAs (1.2 V), 6.35-Gbps transceivers[1]		
	FBGA (F)		
	780 pin 29 x 29 (mm) 1.0 mm pitch	1,152 pin 35 x 35 (mm) 1.0 mm pitch	1,508 pin 40 x 40 (mm) 1.0 mm pitch
EP2SGX30	361 8		
EP2SGX60	364 8	534 12	
EP2SGX90		558 12	650 16
EP2SGX130			734 20

[1] I/O counts do not include dedicated clock inputs that can be used as data inputs.

636
12 Values on top indicate available user I/O pins; values on bottom indicate the 6.35-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚ to 100˚).

HardCopy Series

ALTERA

HardCopy IV ASIC Features

		HardCopy IV ASICs (0.9 V) with 6.5-Gbps Transceiver Option				
		HC4GX15	HC4GX25	HC4GX35	HC4E25	HC4E35
Density and Speed	Usable ASIC gates	9.4M	11.5M	11.5M	9.4M	15M
	Equivalent LEs	353,600	531,600	531,600	353,600	813,050
	M9K memory blocks	660	936	1,280	864	1,320
	M144K memory blocks	24	36	64	32	48
	MLAB memory	Implemented in HCells				
	Embedded memory (Kb)	9,396	13,608	20,736	12,384	18,792
	18-bit x 18-bit multipliers[1]	1,288	1,288	1,288	1,288	1,040
Architectural Features	PLLs/unique outputs	3/27	6/54	8/68	4/34	12/96
	Design security[2]	✓				
	Stratix series prototyping support	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX360	EP4SGX110 EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530	EP4SE230 EP4SE360	EP4SE360 EP4SE530 EP4SE820
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2,Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)				
	Emulated LVDS channels 1,100 Mbps	184	236	280	120	216
	LVDS channels, 1,250 Mbps (receive/transmit)	28/28	44/44	88/88	56/56	88/88
	Embedded DPA circuitry	✓				
	Series and differential OCT	✓				
	Transceiver (SERDES) channels, 6.5 Gbps/6.5 Gbps PMA only	8/0	16/8	24/12	—	—
	PCIe hard IP blocks	1	2	2	—	—
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR				

[1]Implemented in HCells.
[2]Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

HardCopy III ASIC Features

		HardCopy III ASICs (0.9 V)	
		HC325	HC335
Density and Speed	Usable ASIC gates	7.0M	7.0M
	Equivalent LEs	338,000	338,000
	M9K memory blocks	864	1,040
	M144K memory blocks	32	48
	MLAB memory	Implemented in HCells	
	Embedded memory (Kb)	12,384	16,272
	18-bit x 18-bit multipliers[1]	896	
Architecural Features	PLLs/unique outputs	8/68	12/96
	Design security[2]		
	Stratix series prototyping support	EP3SE110 EP3SL110 EP3SL150 EP3SL200 EP3SE260 EP3SL340	EP3SE110 EP3SL150 EP3SL200 EP3SE260 EP3SL340
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	Emulated LVDS channels 1,100 Mbps	120	216
	LVDS channels, 1,250 Mbps (receive/transmit)	56/56	88/88
	Embedded DPA circuitry	✓	✓
	Series and differential OCT	✓	
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR	

[1]Implemented in HCells.
[2]Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

HardCopy Series

ALTERA

HardCopy II ASIC Features

		HardCopy II ASICs					
		HC210W	HC210	HC220W	HC220	HC230	HC240
Density and Speed	Usable ASIC gates	1.0M	1.0M	1.9M	1.9M	2.9M	3.6M
	Equivalent LEs	90,960	90,960	90,960	132,540	179,400	179,400
	M512 memory blocks	Not available in HardCopy II ASICs					
	M4K memory blocks	190	190	408	408	614	768
	M512K memory blocks	0	0	2	2	6	9
	Embedded memory (Kb)	855	855	2,988	2,988	6,219	8,640
	18-bit x 18-bit multipliers[1]	192	192	252	252	384	384
Architectural Features	PLLs/unique outputs	4/32	4/32	4/32	4/32	8/64	12/88
	Design security[2]	✓					
	Stratix series prototyping support	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S60	EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180
I/O Features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X 1.0, LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HyperTransport					
	Emulated LVDS channels, 340 Mbps	Contact Altera					
	LVDS channels, 1,040 Mbps (receive/transmit)	17/13	21/19	26/24	30/29	46/44	116/116
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
External Memory Interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] Implemented in HCells.
[2] Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

HardCopy Series Package and I/O Matrices

	HardCopy IV ASICs (0.9 V), 6.5-Gbps Transceivers								
	FBGA (F)								
	484 (WF[1]) 23 x 23 (mm) 1.0 mm pitch	484 (FF[2]) 23 x 23 (mm) 1.0 mm pitch	780 (WF) 29 x 29 (mm) 1.0 mm pitch	780 (LF[3]) 29 x 29 (mm) 1.0 mm pitch	780 (FF) 29 x 29 (mm) 1.0 mm pitch	1,152 (LF) 35 x 35 (mm) 1.0 mm pitch	1,152 (FF) 35 x 35 (mm) 1.0 mm pitch	1,517 (LF) 40 x 40 (mm) 1.0 mm pitch	1,517 (FF) 40 x 40 (mm) 1.0 mm pitch
HC4GX15				372 8+0					
HC4GX25				289 16+0		564 16+0	564 16+8		
HC4GX35							564 16+8		744 24+12
HC4E25	296	296	392		488				
HC4E35						744	744	880	880

636 / 8+0 Values on top indicate available user I/O pins; values at the bottom indicate the 6.5-Gbps physical media attachment (PMA) and physical coding sublayer (PCS) plus the 6.5-Gbps PMA-only transceiver count.

All HardCopy series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

	HardCopy III ASICs (0.9 V)							
	FBGA (F)							
	484 (WF) 23 x 23 (mm) 1.0 mm pitch	484 (FF) 23 x 23 (mm) 1.0 mm pitch	780 (WF) 29 x 29 (mm) 1.0 mm pitch	780 (FF) 29 x 29 (mm) 1.0 mm pitch	1,152 (LF) 35 x 35 (mm) 1.0 mm pitch	1,152 (FF) 35 x 35 (mm) 1.0 mm pitch	1,517 (LF) 40 x 40 (mm) 1.0 mm pitch	1,517 (FF) 40 x 40 (mm) 1.0 mm pitch
HC325	296	296	392	488				
HC335					744	744	880	880

636 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

	HardCopy II ASICs (0.9 V)							
	FBGA (F)							
	484 (WF) 23 x 23 (mm) 1.0 mm pitch	484 (F[4]) 23 x 23 (mm) 1.0 mm pitch	672 (WF) 27 x 27 (mm) 1.0 mm pitch	672 (F) 27 x 27 (mm) 1.0 mm pitch	780 (WF) 29 x 29 (mm) 1.0 mm pitch	780 (F) 29 x 29 (mm) 1.0 mm pitch	1,020 (F) 33 x 33 (mm) 1.0 mm pitch	1,508 (F) 40 x 40 (mm) 1.0 mm pitch
HC210W	308							
HC210		334						
HC220W			442		444			
HC220				492		494		
HC230							698	
HC240							742	951

[1] WF = Wire bond.
[2] FF = Performance-optimized flip chip.
[3] LF = Cost-optimized flip chip.
[4] F= Performance-optimized flip chip.

636 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

Arria Series

ALTERA

Arria II GX FPGA Features

		Arria II GX FPGAs (0.9 V), Up to 6.375-Gbps Transceivers[1]					
		EP2AGX45	EP2AGX65	EP2AGX95	EP2AGX125	EP2AGX190	EP2AGX260
Density and Speed	ALMs	18,050	25,300	37,470	49,640	76,120	102,600
	Equivalent LEs	45,125	63,250	93,675	124,100	190,300	256,500
	Registers[2]	36,100	50,600	74,940	99,280	152,240	205,200
	M9K memory blocks	319	495	612	730	840	950
	MLAB memory (Kb)	564	791	1,171	1,551	2,379	3,206
	Embedded memory (Kb)	2,871	4,455	5,508	6,570	7,560	8,550
	18-bit x 18-bit embedded multipliers	232	312	448	576	656	736
	Speed grades (fastest to slowest)	-4, -5, -6					
Architectural Features	Global clock networks	16					
	Regional clock networks	48					
	Periphery clock networks	50	50	59	59	84	84
	PLLs/unique outputs	4/28	4/28	6/42	6/42	6/42	6/42
	Configuration file size (Mb)	18	18	34	34	64	64
	Design security	✓					
	Others	Plug & Play Signal Integrity					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	Emulated LVDS channels, 840 Mbps	56	56	64	64	96	96
	LVDS channels, 1,000 Mbps (receive/transmit)	85/84	85/84	105/104	105/104	145/144	145/144
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
	Transceiver (SERDES) channels	8	8	12	12	16	16
	PCIe hard IP block Gen1	1					
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II					

[1] Maximum 18-bit x 18-bit embedded multipliers, LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety of options to meet your design needs.

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

Arria II GZ FPGA Features

		Arria II GZ FPGAs (0.9 V), 6.375-Gbps Transceivers[1]		
		EP2AGX225	EP2AGX300	EP2AGX350
Density and Speed	ALMs	89,600	119,200	139,400
	Equivalent LEs	224,000	298,000	348,500
	Registers	179,200	238,400	278,800
	M9K memory blocks	1,235	1,248	1,248
	M144K memory blocks	0	24	36
	MLAB memory (Kb)	2,800	3,725	4,356
	Embedded memory (Kb)	11.1	14.7	16.4
	18-bit x 18-bit embedded multipliers	700	920	1,040
	Speed grades (fastest to slowest)	-3, -4		
Architectural Features	Global clock networks	16		
	Regional clock networks	64	88	88
	Periphery clock networks	88		
	PLLs/unique outputs	8/68	12/96	12/96
	Configuration file size (Mb)	95	141	141
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]		
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.8-V (I and II)		
	Emulated LVDS channels	192	256	256
	Emulated LVDS channels, 1,250 Mbps	192		
	LVDS channels, 1250 Mbps (receive/transmit)	88		
	Embedded DPA circuitry	✓		
	Series and differential OCT	✓		
	Transceiver (SERDES) channels, 6.375 Gbps	24		
	PCIe hard IP block (value as 1.1, 2.0, etc)	1		
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR		

[1] Maximum 18-bit x 18-bit embedded multipliers, LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety of options to meet your design needs.

[2] 3.3 V compliant, requires a 3-V power supply.

Arria II GX FPGA Package and I/O Matrices

	Arria II GX FPGAs (0.9 V), 6.375-Gbps Transceivers			
	UBGA (U)[1]	FBGA (F)		
	358 pin 17 x 17 (mm) 0.8 mm pitch	**572 pin** 25 x 25 (mm) 1.0 mm pitch	**780 pin** 29 x 29 (mm) 1.0 mm pitch	**1,152 pin** 35 x 35 (mm) 1.0 mm pitch
EP2AGX45	156 4	252 8	364 8	
EP2AGX65	156 4	252 8	364 8	
EP2AGX95		260 8	372 12	452 12
EP2AGX125		260 8	372 12	452 12
EP2AGX190			372 12	612 16
EP2AGX260			372 12	612 16

[1]Ultra-FineLine ball grid array

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 3.75-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Arria II GZ FPGAs (0.9 V), 6.375-Gbps Transceivers		
	Hybrid FBGA (H)		FBGA (F)
	1,152 pin 35 x 35 (mm) 1.0 mm pitch	**1,517 pin** 40 x 40 (mm) 1.0 mm pitch	**780 pin** 33 x 33 (mm) 1.0 mm pitch
EP2AGZ225	550 16	726 16	
EP2AGZ300	550 16	726 16	278 16
EP2AGZ350	550 24	726 16	278 24

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate 3.75-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone Series

ALTERA

Cyclone IV GX FPGA Features

		Cyclone IV GX FPGAs (1.2 V), 3.125-Gbps Transceivers[1]						
		EP4CGX15	EP4CGX22	EP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150
Density and Speed	LEs	14,400	21,280	29,440	49,888	73,920	109,424	149,760
	M9K memory blocks	60	84	120	278	462	666	720
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480
	18-bit x 18-bit multipliers	0	40	80	140	198	280	360
	Speed grades (fastest to slowest)	-6,-7,-8	-6,-7,-8	-6,-7,-8	-6,-7,-8	-6,-7,-8	-7,-8	-7,-8
Architectural Features	Global clock networks	20	20	20	30	30	30	30
	PLLs/unique outputs	3/15	4/20	4/20	8/40	8/40	8/40	8/40
	Configuration file size (Mb)	3.8	7.6	7.6	24.5	24.5	47.6	47.6
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)						
	Emulated LVDS channels	9	40	40	73	73	139	139
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59
	Transceiver (SERDES) channels (2.5/3.125 Gbps)	2/0	4/0	4/0	0/8	0/8	0/8	0/8
	PCIe hard IP blocks Gen1	1						
External Memory Interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR						

[1]Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety options to meet your design needs.

Cyclone IV E FPGA Features

		Cyclone IV E FPGAs								
		EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Density and Speed	LEs	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
	M9K memory blocks	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	270	414	504	594	594	1,134	2,340	2,745	3,888
	18-bit x 18-bit multipliers	15	23	56	66	66	116	154	200	266
	Speed grades (fastest to slowest)	6, 7, 8 -8L, -9L	6, 7, 8 8L, 9L	6, 7, 8 8L, 9L	6, 7, 8 8L, 9L	6, 7, 8 8L, 9L	6, 7, 8 8L, 9L	6, 7, 8 8L, 9L	6, 7, 8 8L, 9L	7, 8 8L, 9L
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mb)	2.8	2.8	3.9	5.5	9.1	9.1	14.2	19	27.2
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3								
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)								
	LVDS channels	66	66	136	52	227	227	163	181	233
External Memory Interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR								

Cyclone Series

ALTERA

Cyclone III FPGA Features

		Cyclone III FPGAs (1.2 V)							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Density and Speed	LEs	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
	M9K memory blocks	46	46	56	66	126	260	305	432
	Embedded memory (Kb)	414	414	504	594	1,134	2,340	2,745	3,888
	18-bit x 18-bit embedded multipliers	23	23	56	66	126	156	244	288
	Speed grades (fastest to slowest)[1]	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-7, -8
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mb)	2.8	2.8	3.9	5.5	9.1	14.2	19	27.2
	Design security	✓							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS							
	Emulated LVDS channels, 840 Mbps	66	66	136	79	223	159	177	229
	Series and differential OCT	✓							
	Programmable drive strength	✓							
External Memory Interfaces	Memory device supported	QDR II, DDR2, DDR, SDR							

[1]Not all packages are supported in all speed grades.

Cyclone III FPGA Features

		Cyclone III LS FPGAs (1.2 V)			
		EP3CLS70	EP3CLS100	EP3CLS150	EP3CLS200
Density and Speed	LEs	70,208	100,488	150,848	198,464
	M9K memory blocks	333	483	666	891
	Embedded memory (Kb)	2,997	4,347	5,994	8,019
	18-bit x 18-bit embedded multipliers	200	276	320	396
	Speed grades (fastest to slowest)[1]	-7, -8			
Architectural Features	Global clock networks	20			
	PLLs/unique outputs	4/20			
	Configuration file size (Mb)	26.8	26.8	50.6	50.6
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	LVDS channels, 840 Mbps	169			
	Series and differential OCT	✓			
External Memory Interfaces	Memory device supported	QDR II, DDR2, DDR, SDR			

[1]Not all packages are supported in all speed grades.

Cyclone Series

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Cyclone Series Package and I/O Matrices

	Cyclone IV GX FPGAs (1.2 V), Up to 3.125-Gbps Transceivers					
	QFN (N)	FBGA (F)				
	148 pin 11 x 11 (mm) 0.5 mm pitch	169 pin 14 x 14 (mm) 1.0 mm pitch	324 pin 19 x 19 (mm) 1.0 mm pitch	484 pin 23 x 23 (mm) 1.0 mm pitch	672 pin 27 x 27 (mm) 1.0 mm pitch	896 pin 31 x 31 (mm) 1.0 mm pitch
EP4CGX15	72 2	72 2				
EP4CGX22		72 2	150 4			
EP4CGX30		72 2	150 4			
EP4CGX50				290 4	310 8	
EP4CGX75				290 4	310 8	
EP4CGX110				270 4	393 8	475 8
EP4CGX150				270 4	393 8	475 8

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 2.5-Gbps or 3.125-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Cyclone IV E FPGAs (1.0 V and 1.2 V)			
	EQFP (E)[1]	FBGA (F)		
	144 pin 22 x 22 (mm) 0.5 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch	484 pin 23 x 23 (mm) 1.0 mm pitch	780 pin 29 x 29 (mm) 1.0 mm pitch
EP4CE6	91	179		
EP4CE10	91	179		
EP4CE15	81	165	343	
EP4CE22	79	153		
EP4CE30			328	532
EP4CE40			328	532
EP4CE55			324	374
EP4CE75			292	426
EP4CE115			280	528

[1] Enhanced thin quad flat pack

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Cyclone III FPGAs (1.2 V)								
	EQFP1 (E)	MBGA (M)[1]	PQFP (Q)[2]	FBGA (F)				UBGA (U)	
	144 pin 22 x 22 (mm) 0.5 mm pitch	164 pin 8 x 8 (mm) 0.5 mm pitch	240 pin 34.6 x 34.6 (mm) 0.5 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch	324 pin 19 x 19 (mm) 1.0 mm pitch	484 pin 23 x 23 (mm) 1.0 mm pitch	780 pin 29 x 29 (mm) 1.0 mm pitch	256 pin 14 x 14 (mm) 0.8 mm pitch	484 pin 19 x 19 (mm) 0.8 mm pitch
EP3C5	94	106		182				182	
EP3C10	94	106		182				182	
EP3C16	84	92	160	168		346		168	346
EP3C25	82		148	156	215			156	
EP3C40			128		195	331	535		331
EP3C55						327	377		327
EP3C80						295	429		295
EP3C120						283	531		
EP3CLS70						278	413		278
EP3CLS100						278	413		278
EP3CLS150						210	413		
EP3CLS200						210	413		

[1] Micro FineLine BGA.

[2] Plastic quad flat pack.

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

MAX® Series

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MAX II FPGA Features

		MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)			
		EPM240/Z	EPM570/Z	EPM1270	EPM2210
Density and Speed	Equivalent macrocells[1]	192	440	980	1,700
	Pin-to-pin delay (ns)	4.7, 7.5	5.4, 9.0	6.2	7.0
Architectural Features	User flash memory (Kb)	8			
	Boundary scan JTAG	✓			
	JTAG ISP	✓			
	Fast input registers	✓			
	Programmable register power up	✓			
	JTAG translator	✓			
	Real-time ISP	✓			
I/O Features	MultiVolt I/Os (V)	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3, 5.0[2]	1.5, 1.8, 2.5, 3.3, 5.0[2]
	I/O power banks	2	2	4	4
	Maximum output enables	80	160	212	272
	LVTTL/LVCMOS	✓			
	32-bit, 66-MHz PCI compliant	-	-	✓[2]	✓[2]
	Schmitt triggers	✓			
	Programmable slew rate	✓			
	Programmable pull-up resistors	✓			
	Programmable ground pins	✓			
	Open-drain outputs	✓			
	Bus hold	✓			

[1] Typical equivalent macrocells.
[2] An external resistor must be used for a 5-V tolerance.

MAX 7000AE and 3000A CPLD Features

		MAX 7000AE CPLDs (3.3 V)				
		EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Density and Speed	Macrocells	32	64	128	256	512
	Equivalent LEs	40	80	160	320	640
	Pin-to-pin delay (ns)	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	5.5, 7.5, 10	7.5, 10, 12
Architectural Features	Boundary scan JTAG	✓				
	JTAG ISP	✓				
	Fast input registers	✓				
	Programmable register power up	✓				
I/O Features	MultiVolt I/Os (V)	2.5, 3.3, 5.0				
	I/O power banks	1				
	Maximum output enables	6	6	6	6	10
	LVTTL/LVCMOS	✓				
	Programmable slew rate	✓				
	Open-drain outputs	✓				

		MAX 3000A CPLDs (3.3 V)				
		EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A
Density and Speed	Macrocells	32	64	128	256	512
	Equivalent LEs	40	80	160	320	640
	Pin-to-pin delay (ns)	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	7.5, 10	7.5, 10
Architectural Features	Boundary scan JTAG	✓				
	JTAG ISP	✓				
	Fast input registers	✓				
	Programmable register power up	✓				
I/O Features	MultiVolt I/Os (V)	2.5, 3.3, 5.0				
	I/O power banks	1				
	Maximum output enables	6	6	6	6	10
	LVTTL/LVCMOS	✓				
	Programmable slew rate	✓				
	Open-drain outputs	✓				

MAX® Series

ALTERA®

MAX Series Package and I/O Matrices

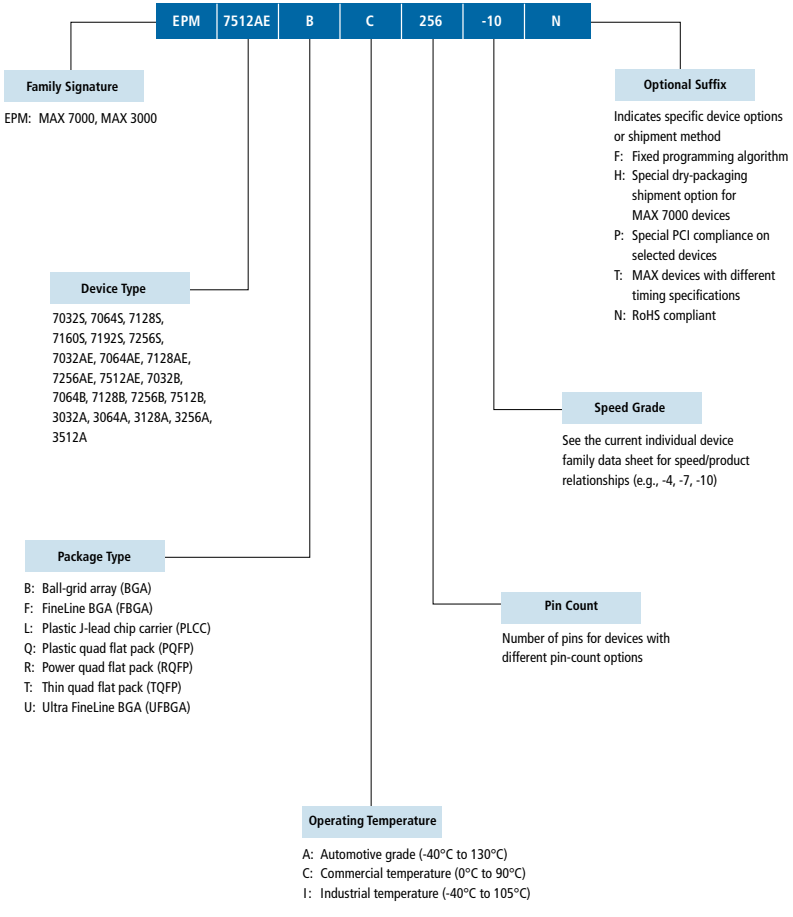
	MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)[1]								
	TQFP (T)[2]		FBGA (F)			MBGA (M)[3]			
	100 pin 16 x 16 (mm) 0.5 mm pitch	144 pin 22 x 22 (mm) 0.5 mm pitch	100 pin 11 x 11 (mm) 1.0 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch	324 pin 16 x 16 (mm) 0.5 mm pitch	68 pin 5 x 5 (mm) 0.5 mm pitch	100 pin 6 x 6 (mm) 0.5 mm pitch	144 pin 7 x 7 (mm) 0.5 mm pitch	256 pin 11 x 11 (mm) 0.5 mm pitch
EPM240Z						54	80		
EPM570Z							76	116	160
EPM240	80		80				80		
EPM570	76	116	76	160			76		160
EPM1270		116		212					212
EPM2210				204	272				

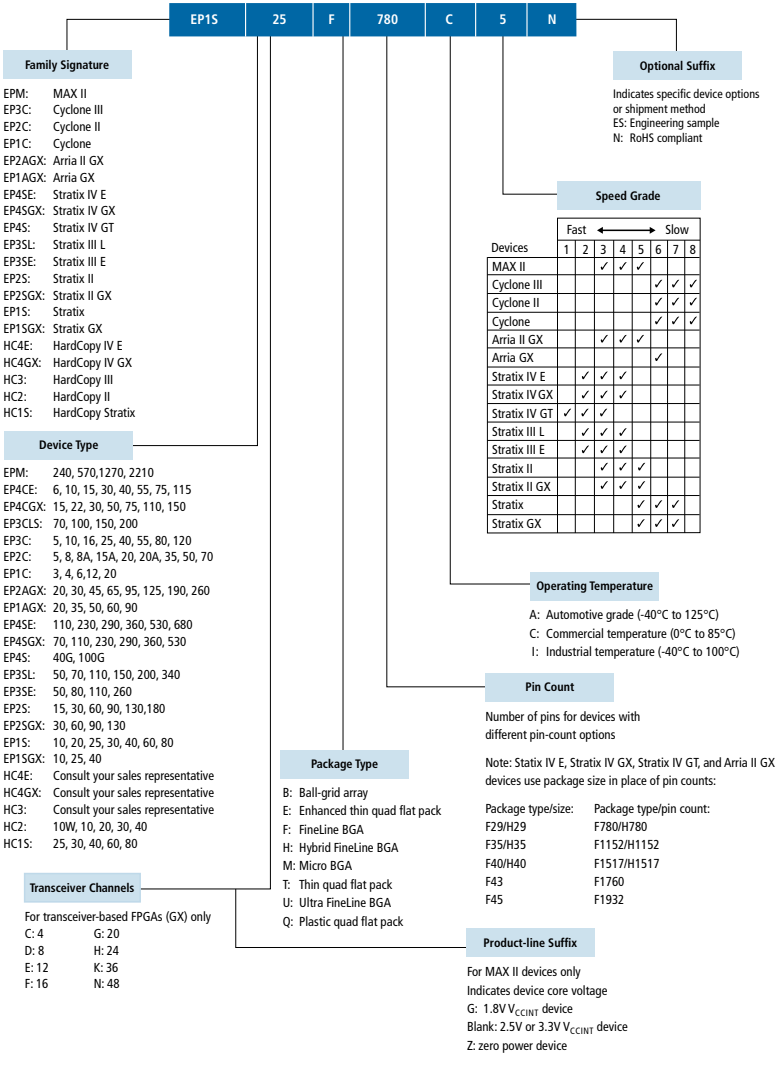
	MAX 7000AE CPLDs (3.3 V)						
	PLCC (L)[4]		TQFP (T)			FBGA (F)	
	44 pin 17.5 x 17.5 (mm) 1.27 mm pitch	84 pin 30 x 30 (mm) 1.27 mm pitch	44 pin 12 x 12 (mm) 0.5 mm pitch	100 pin 16 x 16 (mm) 0.5 mm pitch	144 pin 22 x 22 (mm) 0.5 mm pitch	100 pin 11 x 11 (mm) 1.0 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch
EPM7032AE	36		36				
EPM7064AE	36		36	68		68	
EPM7128AE		68		84	100	84	100
EPM7256AE				84	120	84	164
EPM7512AE					120		212

	MAX 3000A CPLDs (3.3 V)				
	PLCC (L)	TQFP (T)			FBGA (F)
	44 pin 17.5 x 17.5 (mm) 1.27 mm pitch	44 pin 12 x 12 (mm) 0.5 mm pitch	100 pin 16 x 16 (mm) 0.5 mm pitch	144 pin 22 x 22 (mm) 0.5 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch
EPM3032A	34	34			
EPM3064A	34	34	66		
EPM3128A			80	96	98
EPM3256A				116	161
EPM3512A					208

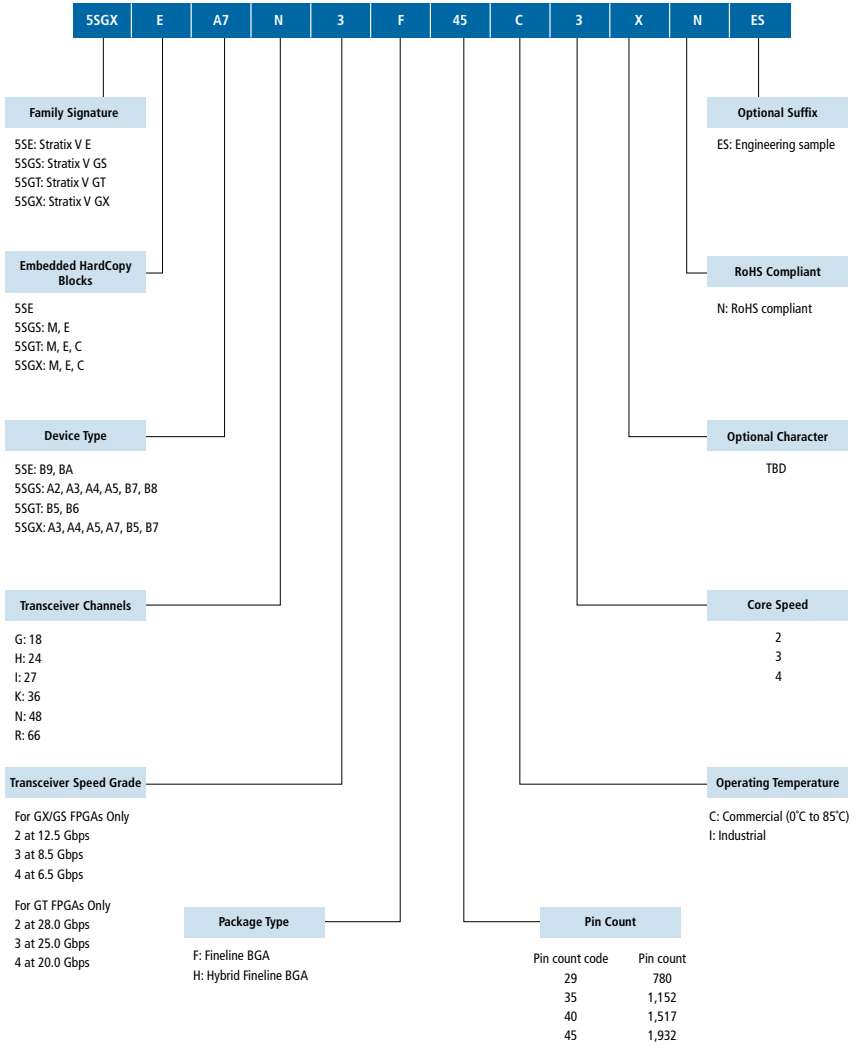
[1] For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Altera's online selector guide.
[2] Thin quad flat pack.
[3] Micro FineLine BGA (0.5 mm).
[4] Plastic J-lead chip carrier.

Ordering Codes





Ordering Codes



Glossary

Below is a glossary of helpful terms to bring you up to speed on Altera devices.

Term	Definition
Adaptive logic module (ALM)	Logic building block, used by some Altera devices, which provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two combinational adaptive LUTs (ALUTs).
Configuration via PCIe (CvPCIe)	This capability enables you to configure the FPGA using the existing PCI Express® (PCIe®) link in your application, reducing configuration time to under 100 ms.
Embedded HardCopy Blocks	These metal-programmable hard IP blocks deliver up to 14M ASIC gates or up to 700K additional logic elements (LEs) to harden standard or logic-intensive applications.
Equivalent LE	Device density represented as a comparable amount of LEs, which uses the 4-input look-up table as a basis.
Fractional phase-locked loops (fPLL)	A phase-locked loop (PLL) in the core fabric, fPLLs provide increased flexibility as an additional clocking source for the transceiver, replacing external voltage-controlled crystal oscillators (VCXOs).
Global clock networks	Global clocks can drive throughout the entire device, serving as low-skew clock sources for functional blocks such as ALMs, DSP blocks, TriMatrix memory blocks, and PLLs. See regional clocks and periphery clocks for more clock network information.
LE	Logic building block, used by some Altera devices, that includes a 4-input LUT, programmable register, and a carry chain connection. See device handbooks for more information.
Macrocells	Similar to logic elements, this is the measure of density in MAX series CPLDs.
Memory logic array blocks (MLABs)	MLABs are dual-purpose blocks, configurable as regular logic array blocks or as memory blocks.
On-chip termination (OCT)	Support for driver impedance matching and series termination, which eliminates the need for external resistors, improves signal integrity, and simplifies board design. On-chip series, parallel, and differential termination resistors are configurable via Quartus II software.
Periphery clocks (PCLKs)	PCLKs are a collection of individual clock networks driven from the periphery of the device. PCLKs can be used instead of general-purpose routing to drive signals into and out of the device.
Plug & Play Signal Integrity	This capability, consisting of Altera's adaptive dispersion engine and hot socketing, let you change the position of backplane cards on the fly, without having to manually configure your backplane equalization settings.
Programmable Power Technology	This feature automatically optimizes logic, DSP, and memory blocks for the lowest power at the required performance. Only the blocks with critical-path logic need to be in high-performance mode; all others are in low-power mode.
Real-time in-system programming (ISP)	This capability allows you to program a MAX II device while the device is still in operation. The new design only replaces the existing design when there is a power cycle to the device. This way, you can perform in-field updates to the MAX II device at any time without affecting the operation of the whole system.
Regional clocks	Regional clocks are device quadrant-oriented and provide the lowest clock delay and skew for logic contained within a single device quadrant.
Variable-precision DSP blocks	These integrated blocks provide native support for signal processing of varying precisions—for example, 9x9, 27x27, and 18x36—in a sum or independent mode.