VHDL VITAL™
Simulation Guide
R1-2003

Windows® and UNIX® Environments

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Table of Contents

Introduction 5
Document Organization 5
Document Assumptions 6
Document Conventions 6
Your Comments 7
Actel Manuals 7
Online Help 7

1 Setup 9
Software Requirements 9
Project Setup for Viewlogic SpeedWave (PC Only) 15

2 Design Flow 19
VHDL VITAL Design Flow Illustrated 19
VHDL VITAL Design Flow Described 20

3 Generating Netlists 23
Generating an EDIF Netlist 23
Generating a Structural VHDL Netlist 23

4 Simulation with ModelSim 25
Behavioral Simulation 25
Structural Simulation 27
Timing Simulation 28

5 Simulation with Cadence NC-VHDL 31
Behavioral Simulation 31
Structural Simulation 32
Timing Simulation 34

6 Simulation with Innoveda SpeedWave 37
Behavioral Simulation (PC) 37
Structural Simulation (PC) 38

Timing Simulation (PC) 39
Behavioral Simulation (UNIX) 41
Structural Simulation (UNIX) 42
Timing Simulation (UNIX) 44

7 Simulation with Synopsys VSS .45
Behavioral Simulation 45
Structural Simulation. 46
Timing Simulation 46

A Product Support 49
Actel U.S. Toll-Free Line 49
Customer Service 49
Actel Customer Technical Support Center 49
Guru Automated Technical Support .50
Web Site 50
Contacting the Customer Technical Support Center 50
Worldwide Sales Offices. 52

Index 53

Introduction

This *VHDL Vital Simulation Guide* contains information about using the Model Technology V-System or ModelSim, Mentor Graphics QuickHDL, Cadence NC-VHDL, Viewlogic SpeedWave, and Synopsys VSS to simulate designs for Actel devices. Refer to the *Designer User's Guide* for additional information about using the Designer software. Refer to the documentation included with your simulator for information about performing simulation.

Document Organization

The *VHDL Vital Simulation Guide* contains the following sections:

Chapter 1 - Setup contains information about setting up Model Technology's V-System or ModelSim simulator, the Mentor Graphics QuickHDL simulator, the Cadence Leapfrog simulator, the Viewlogic SpeedWave simulator, and the Synopsys VSS simulator.

Chapter 2 - Design Flow describes how to use the VHDL design flow to design an Actel device using Synopsys, or other synthesis-tool software, and VHDL simulator software.

Chapter 3 - Generating Netlists contains information regarding how to generate a netlist using Synopsys or other synthesis-tool software.

Chapter 4 - Simulation with ModelSim contains information about simulating for Actel designs using the Model Technology's V-System or ModelSim simulator.

Chapter 5 - Simulation with Cadence NC-VHDL contains information about simulating for Actel designs using the Cadence NC-VHDL simulator.

Chapter 6 - Simulation with Innoveda SpeedWave contains information about simulating for Actel designs using the Viewlogic SpeedWave simulator.

Chapter 7 - Simulation with Synopsys VSS contains information about simulating for Actel designs using the Synopsys VSS simulator.

Appendix A - Product Support provides information regarding contacting Actel for customer and technical support.

Document Assumptions

This document assumes the following:

1. You have installed the Designer Series software.
2. You have installed your VHDL VITAL simulator.
3. You are familiar with UNIX workstations and operating systems or with PCs and Windows operating environments.
4. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

This document uses the following conventions:

Information input by the user follows this format:

```
keyboard input
```

The contents of a file follows this format:

```
file contents
```

This document uses the following variables:

- Actel FPGA family libraries are shown as <act_fam>. Substitute the desired Actel FPGA family ACT1, ACT2 (for ACT 2 and 1200XL devices), ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, eX, A500K and APA as needed. For example:

  ```
  edn2vhdl fam:<act_fam> <design_name>
  ```

- Compiled VHDL libraries are shown as <vhd_fam>. Substitute <vhd_fam> for the desired VHDL family ACT1, ACT2 (for ACT 2 and 1200XL devices), ACT3, A3200DX, A40MX, A42MX, A54SX, A54SX-A, eX, A500K, or APA as needed. The VHDL language requires that the library names begin with an alpha character.

Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products, so you can get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **documentation@actel.com**.

Actel Manuals

Designer and Libero include printed and online manuals. The online manuals are in PDF format and available from Libero and Designer's Start Menus and on the CD-ROM. From the Start menu choose:

- Programs > Libero x.x > Libero x.x Documentation.
- Programs > Designer Series > R1-2003 Documentation

Also, the online manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

Online Help

The Designer Series software comes with online help. Online help specific to each software tool is available in Libero, Designer, ACTgen, ACTmap, Silicon Expert, Silicon Explorer II, Silicon Sculptor, and APSW.

1

Setup

This chapter contains information on setting up the Model Sim, Cadence NC-VHDL, Viewlogic SpeedWave, or Synopsys VSS simulator to simulate Actel designs.

This chapter includes software requirements, steps describing how to compile Actel FPGA libraries, and other setup information for the simulation tool you use.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R1-2003 or later and IEEE-1076-compliant VHDL simulators. Additionally, this guide contains information about using Model Sim, Cadence NC-VHDL, Viewlogic SpeedWave, and Synopsys VSS and VeriBest simulators.

For specific information about which versions this release supports, go to the Guru automated technical support system on the Actel web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

Migration Libraries

In addition to the standard Actel libraries, Actel provides a set of migration libraries. These libraries contain macros supported in 3.1.1u1 and earlier versions of the Designer Series software and macros possibly needed to retarget designs from a different Actel family. Actel does not recommend using the migration libraries on new designs.

ModelSim

Use the following procedure to compile libraries for the ModelSim simulators. Type UNIX commands at the UNIX prompt. Type PC commands on the command line of the ModelSim Transcript window. The commands below are for PC. To make the commands work for UNIX, use forward slashes instead of back slashes.

This procedure compiles an Actel VITAL library in the "$ALSDIR\lib\vtl\95\mti" directory. You must compile the FPGA library models for the Actel VITAL 95 libraries to work properly.

Note: If there is already an MTI directory in the $ALSDIR\lib\vtl\95 directory, compiled libraries may be present, and you may not need to perform the following procedure.

1. **Create a directory called "mti" in the "$ALSDIR\lib\vtl\95" directory.**
2. **Invoke the ModelSim simulator (PC only).**
3. **Change to the "$ALSDIR\lib\vtl\95\mti" directory.** Type the following command at the prompt:

   ```
   cd $ALSDIR\lib\vtl\95\mti
   ```

4. **Create a <vhd_fam> family library directory for your simulator.** Type the following command at the prompt:

   ```
   vlib <vhd_fam>
   ```

5. **Map the Actel VITAL libray to the <vhd_fam> directory.** Type the following command at the prompt:

   ```
   vmap <vhd_fam> $ALSDIR\lib\vtl\95\mti\<vhd_fam>
   ```

6. **Compile the library.** Type the following command at the prompt:

   ```
   vcom -work <vhd_fam> ..\<act_fam>.vhd
   ```

   For example, to compile the 40MX library for your simulator, type the following command:

   ```
   vcom -work a40mx ..\40mx.vhd
   ```

7. **(Optional) Compile the migration library**. Only perform this step if you are using the migration library. Type the following command at the prompt:

   ```
   vcom -work <vhd_fam> ..\<act_fam>_mig.vhd
   ```

Cadence NC-VHDL

Use the following procedure to compile libraries for the Cadence NC-VHDL simulator (UNIX only). This procedure compiles an Actel VITAL library in the "$ALSDIR/lib/vtl/95/ncvhdl" directory. You must compile the FPGA library models for the Actel VITAL 95 libraries to work properly.

1. **Create a directory called "ncvhdl" in the "$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "$ALSDIR/lib/vtl/95/ncvhdl" directory.**
3. **Create a directory named <vhd_fam>.**
4. **Map the library.** Compile the models and create the "cds.lib" file as follows:

```
INCLUDE $CDS/tools/inca/files/cds.lib
DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/ncvhdl/<vhd_fam>
```

5. **Compile the library.** Type the following command at the prompt:

```
ncvhdl -work <vhd_fam> -messages $ALSDIR/lib/vtl/95/
<act_fam>.vhd
```

   For example, to compile the 40MX library for your simulator, type the following command:

```
ncvhdl -work a40mx -messages $ALSDIR/lib/vtl/95/40mx.vhd
```

6. **(Optional) Compile the migration library.** Only perform this step if you are using the migration library. Type the following command at the prompt:

```
ncvhdl -work <vhd_fam> -messages $ALSDIR/lib/vtl/95/
<act_fam>_mig.vhd
```

Viewlogic SpeedWave (PC)

Use the following procedure to compile Actel VITAL libraries for the Viewlogic SpeedWave simulator (PC only).

During the installation of the SpeedWave simulator, you can choose to install the Synopsys IEEE library or the Vantage IEEE library. You need the Synopsys library for compatibility with the Actel VITAL libraries. The Synopsys library is a superset of the Vantage library.

1. **Create a directory called "swave" in the "c:\actel\lib\vtl\95" directory.**
2. **Set your project directory.** Invoke Project Manager and click the New button. Enter "swave" in the Project Name box and "c:\actel\lib\vtl\95\swave" in the Project Directory box. Click the Next button three times, then click the Finish button to complete the process. Do not set your library search order.
3. **Save your project and exit Project Manager.**
4. **Invoke SpeedWave.**
5. **Open the HDL Library Manager window.** Choose the Analyze VHDL Design command from the File menu. Click Cancel in the Welcome dialog box. The HDL Manager window is displayed.
6. **Create a <vhd_fam> library.** Choose the Create command from the Library menu. Specify "c:\actel\lib\vtl\95\swave" in the Library Path box and <vhd_fam> in the Symbolic Name box. Click OK.
7. **Add system libraries to search order.** Make sure that the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under the VHDL System Libraries section in the VHDL View window.
8. **Add the Actel VITAL library to the <vhd_fam> library.** Choose the Add Source Files command from the Library menu. Select the <act_fam>.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.
9. **Compile the Actel VITAL library.** Select the <act_fam>.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.
10. **(Optional) Add the Actel VITAL Migration library to the <vhd_fam> library.** Select the <act_fam>_mig.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.

11. **(Optional) Compile the Actel VITAL Migration library.** Only perform this step if you are using the migration library. Select the <act_fam>_mig.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.

Viewlogic SpeedWave (UNIX)

Use the following procedure to compile libraries for Viewlogic's SpeedWave simulator. This procedure compiles an Actel VITAL library in the "$ALSDIR/lib/vtl/95/swave" directory. You must compile the FPGA library models for the Actel VITAL 95 libraries to work properly.

During the installation of the SpeedWave simulator, you can choose to install the Synopsys IEEE library or the Vantage IEEE library. The Synopsys library is a superset of the Vantage library and you need to use it with the Actel VITAL libraries.

The following procedures use the Vantage IEEE library. To use the Synopsys IEEE library, use the "-lib $VANTAGE_VSS/pgm/libs/synopsys.lib" switch in the "analyze" and "simulation" commands described below.

1. **Create a "swave" directory in the "$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "$ALSDIR/lib/vtl/95/swave" directory.**
3. **Create and map a library directory for your simulator.** Type the following command at the prompt:

```
vanlibcreate $ALSDIR/lib/vtl/95/swave/<vhd_fam> <vhd_fam>
```

4. **Compile the library.** Type the following command at the prompt:

```
analyze -src ../<act_fam>.vhd -lib <vhd_fam> -libieee -lib
$VANTAGE_VSS/pgm/lib/synopsys.lib
```

For example, to compile the 40MX library for your simulator, type the following command:

```
analyze -src ../40mx.vhd -lib a40mx -libieee -lib
$VANTAGE_VSS/pgm/lib/synopsys.lib
```

5. **(Optional) Compile the migration library models.** Type the following command at the prompt:

```
analyze -src ../<act_fam>_mig.vhd -lib <vhd_fam> -libieee
-lib $VANTAGE_VSS/pgm/lib/synopsys.lib
```

Synopsys VSS

Use the following procedures to compile libraries for the Synopsys VSS simulator (UNIX). This procedure compiles an Actel VITAL library in the “$ALSDIR/lib/vtl/95/vss” directory. You must compile the VITAL library models prior to using them to simulate.

1. **Create a “vss” directory in the “$ALSDIR/lib/vtl/95” directory.**
2. **Create a <vhd_fam> directory in the “$ALSDIR/lib/vtl/95/vss” directory.**
3. **Using a text editor, create a “.synopsys_vss.setup” file in the “$ALSDIR/lib/vtl/95/vss” directory.** Type the following command at the prompt:

```
<vhd_fam>: ./<vhd_fam>
default: ./<vhd_fam>
```

4. **Change to the “$ALSDIR/lib/vtl/95/vss” directory and compile the library.** Type the following command at the prompt:

```
cd $ALSDIR/lib/vtl/95/vss
vhdlan -w <vhd_fam> $ALSDIR/lib/vtl/95/<act_fam>.vhd
```

For example, to change to the “$ALSDIR/lib/vtl/95/vss” directory and compile the 40MX library for your simulator, type the following command:

```
cd $ALSDIR/lib/vtl/95/vss
vhdlan -w a40mx $ALSDIR/lib/vtl/95/40mx.vhd
```

5. **(Optional) Change to the “$ALSDIR/lib/vtl/95/vss” directory and compile the migration library.** Only perform this step if you are using the migration library. Type the following command at the prompt:

```
cd $ALSDIR/lib/vtl/95/vss
vhdlan -w <vhd_fam> $ALSDIR/lib/vtl/95/<act_fam>_mig.vhd
```

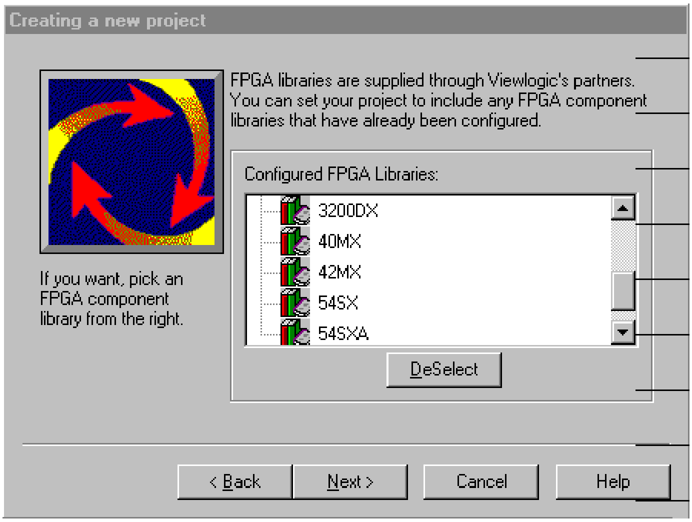
6. **Check for any warning or error messages.**

Project Setup for Viewlogic SpeedWave (PC Only)

You must set up an Actel project in the Viewlogic Project Manager for each Actel design before creating your design in Viewlogic. The following procedures describe the process.

1. **Invoke Project Manager.**
2. **Set up a new project.** Choose the New command from the File menu. The Creating a New Project wizard is displayed.
3. **Set the Project Directory.** Type the full path name of your design directory in the Project Directory box or use the Browse button. Type the name of your project in the Project Name box. Click the Next button.
4. **Locate your project file.** Type the full path name of your project file in the Location of Project File box or use the Browse button. Click the Next button.

5. **Select an Actel FPGA library.** Choose a library in the Configured FPGA Libraries box. Click the icon of the Actel library you want to select, then click Next.



Creating a new project

FPGA libraries are supplied through Viewlogic's partners. You can set your project to include any FPGA component libraries that have already been configured.

If you want, pick an FPGA component library from the right.

Figure 1-1. FPGA Libraries dialog box

6. **(Optional) Add additional libraries.** Click the Add button and type the full path name of the library you want to add. Or, use the Browse button.
7. **Save the project.** Choose the Save command from the File menu.

Creating a Project Library in SpeedWave

If you use SpeedWave to simulate your designs, you must create a project library in SpeedWave, in addition to creating an Actel project in Project Manager, for each VHDL synthesis-based Actel project. The following procedures describe the process.

1. **Invoke SpeedWave.**
2. **Open the HDL Manager window.** Choose the Analyze VHDL Design command from the File menu. Click Cancel in the Welcome dialog box. The HDL Manager window is displayed.

3. **Set up a project.** Choose the Create command from the Library menu. The Create Library dialog box is displayed. Make sure the path in the Library Path box is correct and already exists. Type "user" in the Symbolic Name box and click OK. Make sure the Output window reports no errors.
4. **Verify that the "user" library icon appears under the VHDL User Libraries section in the VHDL View window.**
5. **Add the compiled Actel VITAL library to the Project Libraries.** Choose the Add to Workspace command from the Library menu. The Add Existing Library to Workspace dialog box is displayed. Click the ellipsis box to open the Select Directory dialog box. Browse to the "c:\actel\lib\vtl\95\swave\<vhd_fam>.lib" directory and click OK. Click OK again in the Add Existing Library to Workspace dialog box. If you have not compiled the Actel VITAL library, go to "Viewlogic SpeedWave (PC)" on page 12 for the procedure.

   Note: Only add the <vhd_fam>.lib if you have referenced Actel macros in your VHDL netlist.
6. **Add system libraries to the Project Libraries.** Make sure the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under VHDL System Libraries in the VHDL View window. If they are not present, you must reinstall SpeedWave, making sure to choose the Synopsys IEEE libraries when prompted.
7. **Save the project workspace.** Choose the Save command from the File menu.

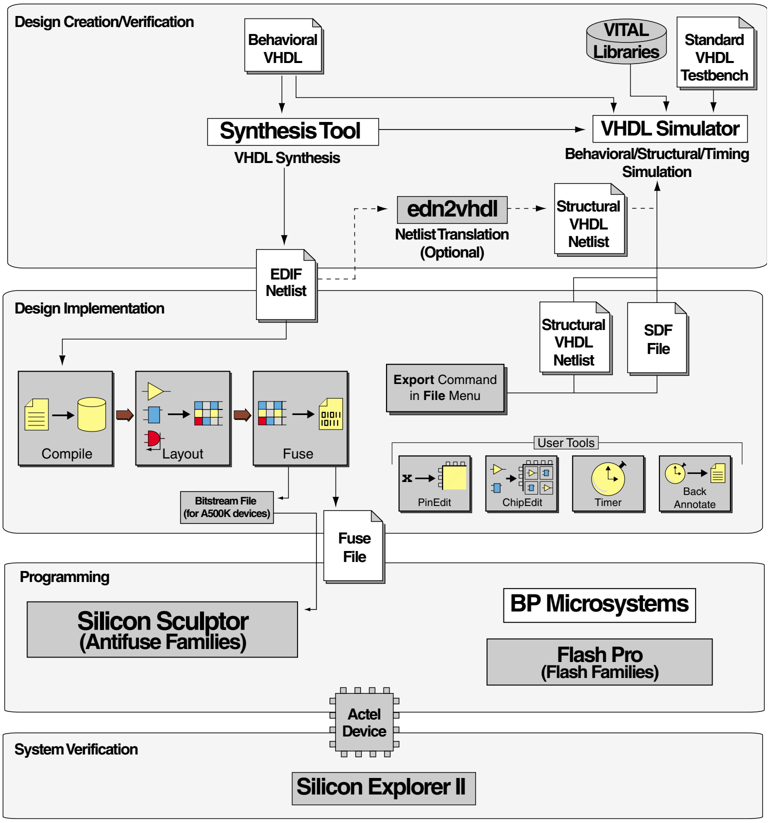
2

Design Flow

This chapter describes the design flow for simulating Actel designs with a VHDL VITAL-compliant simulation tool.

VHDL VITAL Design Flow Illustrated

Figure 2-1 shows the design flow for an Actel FPGA using Designer software and a VITAL-compliant VHDL simulator[1].



Design Creation/Verification
Behavioral VHDL
VITAL Libraries
Standard VHDL Testbench
Synthesis Tool
VHDL Synthesis
VHDL Simulator
Behavioral/Structural/Timing Simulation
edn2vhdl
Netlist Translation (Optional)
Structural VHDL Netlist
EDIF Netlist
Design Implementation
Structural VHDL Netlist
SDF File
Export Command in File Menu
Compile
Layout
Fuse
User Tools
PinEdit
ChipEdit
Timer
Back Annotate
Bitstream File (for A500K devices)
Fuse File
Programming
Silicon Sculptor (Antifuse Families)
BP Microsystems
Flash Pro (Flash Families)
Actel Device
System Verification
Silicon Explorer II

Figure 2-1. Actel-VHDL Design Flow

---

[1] *The grey boxes in Figure 2-1 denote Actel-specific utilities/tools.*

VHDL VITAL Design Flow Described

The Actel VHDL VITAL design flow has four main steps:

1. Design Creation/Verification
2. Design Implementation
3. Programming
4. System Verification

The following sections detail these steps.

Design Creation/ Verification

During design creation/verification, a design is captured in an RTL-level (behavioral) VHDL source file. After capturing the design, you can perform a behavioral simulation of the VHDL file to verify that the VHDL code is correct. The code is then synthesized into an Actel gate-level (structural) VHDL netlist. After synthesis, you can perform an optional pre-layout structural simulation of the design. Finally, an EDIF netlist is generated for use in Designer and a VHDL structural post-layout netlist is generated for timing simulation in a VHDL VITAL-compliant simulator.

VHDL Source Entry

Enter your VHDL design source using a text editor or a context-sensitive HDL editor. Your VHDL design source can contain RTL-level constructs, as well as instantiations of structural elements, such as ACTgen macros.

Behavioral Simulation

Perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your VHDL code. Typically, you use zero delays and a standard VHDL test bench to drive simulation. Refer to the documentation included with your simulation tool for information about performing functional simulation.

Synthesis

After you have created your behavioral VHDL design source, you must synthesize it. Synthesis transforms the behavioral VHDL file into a gate-level netlist and optimizes the design for a target technology. The documentation included with your synthsis tool contains information about performing design synthesis.

EDIF Netlist Generation

After you have created, synthesized, and verified your design, you must generate an Actel EDIF netlist for place-and-route in Designer.

This EDIF netlist is also used to generate a structural VHDL netlist for use in structural simulation.

Structural VHDL Netlist Generation

Generate a gate-level VHDL netlist from your EDIF netlist for use in post-synthesis pre-layout structural simulation by either exporting it from Designer or by using the Actel "edn2vhdl" program.

Structural Simulation

Perform a structural simulation before placing-and-routing. Structural simulation verifies the functionality of your post-synthesis pre-layout structural VHDL netlist. Unit delays included in the compiled Actel VITAL libraries are used. Refer to the documentation included with your simulation tool for information about performing structural simulation.

Design Implementation

During design implementation, you place-and-route a design using Designer. Additionally, you may perform timing analysis on a design in Designer with the Timer tool. After place-and-route, perform postlayout (timing) simulation with a VHDL VITAL-compliant simulator.

Place-and-Route

Use Designer to place-and-route your design. Refer to the *Designer User's Guide* for information about using Designer.

Timing Analysis

Use the Timer tool in Designer to perform static-timing analysis on your design. Refer to the *Timer User's Guide* for information about using Timer.

Timing Simulation

Perform a timing simulation on your design after placing-and-routing it. Timing simulation verifies that the design meets your timing constraints.

Programming

Program a device with programming software and hardware from Actel or a supported third-party programming system. Refer to the *Designer User's Guide* and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

3

Generating Netlists

This chapter describes the procedures for generating EDIF and structural VHDL netlists.

Generating an EDIF Netlist

After capturing your schematic or synthesizing your design, generate an EDIF netlist from your schematic capture or synthesis tool. Use the EDIF netlist for placing-and-routing in Designer. Refer to the documentation included with your schematic capture or synthesis tool for information about generating an EDIF netlist.

Generating a Structural VHDL Netlist

You can generate a structural VHDL netlist using Designer or the "edn2vhdl" program. Use the structural VHDL netlist for structural and timing simulation.

To generate a structural netlist using Designer,

1. **Invoke Designer.**
2. **Import the EDIF netlist.** Choose the Import Source File command from the File menu. This displays the Import Source dialog box. . Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK. In the EDIF Import Options dialog box, specify Generic as the EDIF flavor.
3. **Export a structural VHDL netlist.** From the File menu, choose Export, then Netlist. This displays the Export Netlist Files dialog box. In the Export Netlist Files dialog box, specify the File name and set the Save As type to VHDL. Click OK.

To generate a structural netlist using "edn2vhdl,"

1. **Change to the directory that contains the VHDL design files.**
2. **Type the following command at the UNIX or DOS prompt:**

```
edn2vhdl FAM:{<act_fam>} [ EDNIN:<Edif_File1>[+<Edif_File2...>] ][ VHDOUT:<Vhdl_File> ]<design_name>
```

The "EDNIN" option specifies the EDIF input file(s). You can specify multiple files with the "+" delimiter between file names. The default EDIF input file is <design_name>.edn. The "VHDOUT" option specifies the VHDL output file names. The default VHDL output file is <design_name>.vhd.

4

Simulation with ModelSim

This chapter describes steps to perform Functional (Behavioral and Structural) and Timing simulation for Actel devices using the ModelSim simulator.

The procedures shown are for PC. The same setup procedures work similarly for UNIX. Use forward slashes in place of back slashes. For PC, type commands into the MTI window. For UNIX, type commands into a UNIX window.

Behavioral Simulation

Use the following procedure to perform a behavioral simulation of a design. Refer to the documentation included with your simulation tool for additional information about performing behavioral simulation.

1. **Invoke your ModelSim simulator. (PC only)**
2. **Change directory to your project directory.** This directory must include your VHDL design files and testbench. Type:

   ```
   cd <project_dir>
   ```

3. **Map to the Actel Library.** If any Actel macros are instantiated in your VHDL source, type the following command to map them to the compiled Actel VITAL library.

   ```
   vmap <vhd_fam> $ALSDIR\lib\vtl\95\mti\<vhd_fam>
   ```

   To reference the Actel family library in your VHDL design files, add the following lines to your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

4. **Create a “work” directory.** Type:

   ```
   vlib work
   ```

5. **Map to the “work” directory.** Type the following command:

```
vmap work .\work
```

6. **Perform a behavioral simulation of your design.** To perform a behavioral simulation using your V-System or ModelSim simulator, compile your VHDL design and testbench files and run a simulation. For hierarchical designs, compile the lower-level design blocks before the higher-level design blocks.

   The following commands demonstrate how to compile VHDL design and testbench files:

   ```
   vcom -93<behavioral>.vhd
   vcom -93<test_bench>.vhd
   ```

   To simulate the design, type:

   ```
   vsim <configuration_name>
   ```

   For example:

   ```
   vsim test_adder_behave
   ```

   The entity-architecture pair specified by the configuration named test_adder_behave in the testbench will be simulated.

Structural Simulation

Use the following procedure to perform structural simulation.

1. **Generate a structural VHDL netlist.**

   If you are using Synopsys Design Compiler, generate a structural VHDL netlist using this tool.

   If you are using other synthesis tools, generate a gate-level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a structural netlist using "edn2vhdl,"

2. **Change to the directory that contains the VHDL design files.**
3. **Type the following command at the UNIX or DOS prompt:**

```
edn2vhdl FAM:{<act_fam>} [ EDNIN:<Edif_File1>[+<Edif_File2...>] ][ VHDOUT:<Vhdl_File> ]<design_name>
```

The "EDNIN" option specifies the EDIF input file(s). You can specify multiple files with the "+" delimiter between file names. The default EDIF input file is <design_name>.edn. The "VHDOUT" option specifies the VHDL output file names. The default VHDL output file is <design_name>.vhd.

To generate a netlist using Designer Series software,

4. **Export a structural VHDL netlist.** From the File menu, choose Export, then Netlist. This displays the Export Netlist Files dialog box. In the Export Netlist Files dialog box, specify the File name and set the Save As type to VHDL. Click OK.

   Note: The VHDL generated by both Designer and the edn2vhdl program will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

5. **Map to the Actel VITAL library.** Run the following command to map the compiled Actel VITAL library.

```
vmap <vhd_fam> $ALSDIR\lib\vtl\95\mti\<vhd_fam>
```

6. **Compile the structural netlist.** Compile your VHDL design and testbench files. The following commands demonstrate how to compile VHDL design and testbench files:

   ```
   vcom -93<structural>.vhd -just e
   vcom -93<structural>.vhd -just a
   vcom <test_bench>.vhd
   ```

   Note: First, the application compiles the entities. Then, it compiles the architectures, as required for VHDL netlists written by some tools.

7. **Run the structural simulation.** To simulate your design, type:

   ```
   vsim <configuration_name>
   ```

   For example:

   ```
   vsim test_adder_structure
   ```

   The entity-architecture pair specified by the configuration named test_adder_structure in the testbench will be simulated.

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place-and-route your design in Designer.** Refer to the *Designer User's Guide* for information about using Designer.
2. **Extract timing information for your design.** From the File menu, click Export. Then, click Timing Files. Choose SDF and click Save (or click Back Annotate). The Back Annotate dialog box is displayed. Create a <design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Compile the structural netlist.** To perform a timing simulation using your V-System or ModelSim simulator, compile your VHDL design and testbench files, if they have not already been compiled for a structural simulation, and run a simulation. The following commands demonstrate how to compile VHDL design and testbench files:

```
vcom <structural>.vhd -just e
vcom <structural>.vhd -just a
vcom <test_bench>.vhd
```

Note: Performing the previous steps compiles the entities first and then the architectures, as required for VHDL netlists written by some tools.

4. **Run the back-annotation simulation using the timing information in the SDF file.** Type:

```
vsim -sdf[max|typ|min] /<region>=<design name>.sdf -c
<configuration_name>
```

The <region> option specifies the region (or path) to an instance in a design where back annotation begins. You can use it to specify a particular FPGA instance in a larger system design or testbench that you wish to back annotate. For example:

```
vsim -sdfmax /uut=adder.sdf -c test_adder_structural
```

In this example, the entity "adder" has been instantiated as instance "uut" in the testbench. The entity-architecture pair specified by the configuration named "test_adder_structural" in the testbench will be simulated using the maximum delays specified in the SDF file.

5

Simulation with Cadence NC-VHDL

This chapter describes steps to perform Functional (Behavioral and Structural) and Timing simulation for Actel devices using the Cadence NC-VHDL simulator.

Behavioral Simulation

After you have coded the VHDL descriptions of the logic blocks, test and debug the design using the NC-VHDL simulator. Use the following procedure to perform behavioral simulation.

1. **Create a work directory and a cds.lib file in the project directory.** At the UNIX prompt, type:

   ```
   mkdir work
   ```

2. **Using a text editor, create a cds.lib file and enter the following lines:**

   ```
   INCLUDE $CDS/tools/inca/files/cds.lib
   ```

3. **Map to the Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, add the following lines to your cds.lib file to map them to the compiled Actel VITAL library.

   ```
   DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/ncvhdl/<vhd_fam>
   DEFINE WORK ./work
   ```

   Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

4. **Compile the VHDL design and testbench files.** Type:

   ```
   ncvhdl -work work -messages <behavioral>.vhd
   ncvhdl -work work -messages <test_bench>.vhd
   ```

5. **Elaborate the design.** Type the following commands at the prompt:

   ```
   ncelab -work work -messages <configuration_name>
   ```

In the above, <configuration_name> is the name of the configuration in the testbench.

For example

```
ncelab -work work -messages test_add_behave
```

The entity-architecture pair specified by the configuration named test_adder_behave in the testbench will be elaborated.

6. **Simulate the design.** Type the following command at the prompt:

```
ncsim -batch -run <configuration_name>
```

In the above, <configuration_name> is the name of the configuration in the testbench.

For example:

```
ncsim -batch -run test_add_behave
```

Structural Simulation

Use the following procedure to perform structural simulation.

1. **Map to the Actel VITAL library.** Create a cds.lib file in the project directory as follows:

```
INCLUDE $CDS/tools/inca/files/cds.lib
DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/ncvhdl/<vhd_fam>
DEFINE WORK ./work
```

2. **Compile the structural netlist.** Compile your VHDL design and testbench files. If you have not already generated a structural netlist, go to “Generating a Structural VHDL Netlist” on page 23. The following commands demonstrate how to compile VHDL design and testbench files:

```
ncvhdl -work work -messages <structural>.vhd
ncvhdl -work work -messages <test_bench>.vhd
```

3. **Elaborate the design.** Type:

```
ncelab -work work -messages <configuration_name>
```

In the above, <configuration_name> is the name of your configuration that binds the testbench entity and architecture.

For example:

```
ncelab -work work -messages test_adder_structure
```

In the example, “test_adder_structure” is the name of configuration for the testbench.

4. **Simulate the design.** Type following at the prompt:

```
ncsim -batch -run <configuration_name>
```

In the above, <configuration_name> is name of the testbench configuration.

For example:

```
ncsim -batch -run test_adder_structure
```

Here the name of the testbench configuration is “test_adder_structure.”

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place-and-route your design in Designer.** Refer to the *Designer User's Guide* for information about using Designer.
2. **Extract timing information for your design.** From the File menu, click Export. Then, click Timing Files. Choose SDF and click Save (or click Back Annotate). The Back Annotate dialog box is displayed. Create a <design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Map Actel VITAL library.** If not already done for structural simulation, create a cds.lib file in the project directory using the following command:

```
INCLUDE $CDS/tools/inca/files/cds.lib
DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/ncvhdl/<vhd_fam>
DEFINE WORK ./work
```

4. **Compile the structural netlist.** Compile your VHDL design and testbench files. If you have not already generated a structural netlist, go to “Generating a Structural VHDL Netlist” on page 23. The following commands demonstrate how to compile VHDL design and testbench files:

```
ncvhdl -work work -messages <structural>.vhd
ncvhdl -work work -messages <test_bench>.vhd
```

5. **Compile the SDF file.** Type:

```
ncsdfc <design_name>.sdf
```

6. **Write an SDF command file.** Using a text editor, create the “<design_name>.sdf_cmd” file. Include the following lines:

```
COMPILED_SDF_FILE = “<design_name>.sdf.x”

SCOPE = <UUT>

MTM_CONTROL = “MINUMUM/TYPICAL/MAXIMUM”
```

In the above, <design_name> is the name of the top-level entity, <UUT> is the instance of the top-level entity in the testbench, and <configuration_name> is the name of your configuration that binds the testbench entity and architecture.

7. **Elaborate the design.** Type:

```
ncelab -work work -messages -sdf_cmd_file
<design_name>.sdf_cmd <configuration_name>
```

For example:

```
ncelab -work work -messages -sdf_cmd_file adder.sdf_cmd
test_adder_structure
```

In the above example, "adder" is the name of the top-level entity, "test_adder_structure" is the name of the configuration for the testbench.

8. **Siumulate the design.** Type the following at the prompt:

```
ncsim -batch -run <configuration_name>
```

In the above, <configuration_name> is the name of the testbench configuration.

For example:

```
ncsim -batch -run test_adder_structure
```

Here the name of the testbench configuration is test_adder_structure.

6

Simulation with Innoveda SpeedWave

This chapter describes the procedures for performing simulations on an Actel design using the Innoveda SpeedWave simulation tool. Refer to the Innoveda documentation for additional information about performing simulation with SpeedWave.

Behavioral Simulation (PC)

Use the following procedures to perform a behavioral simulation of an Actel design on a PC.

1. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 15 for the procedure.
2. **Invoke SpeedWave.**
3. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click Cancel in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 16 for the procedure.
4. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select a .hws file and click Open in the Open dialog box.
5. **Analyze your behavioral VHDL design files and testbench.** Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Add Source Files dialog box is displayed. Select the behavioral VHDL and testbench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your testbench.

6. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double-click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.
7. **Simulate the design**. Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click Apply. Click Close when you have completed your simulation.

Structural Simulation (PC)

Use the following procedures to perform a structural simulation of an Actel design on a PC.

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.
2. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 15 for the procedure.
3. **Invoke SpeedWave.**
4. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click Cancel in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 16 for the procedure.
5. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select a .hws file and click Open in the Open dialog box.
6. **Analyze your structural VHDL netlist and testbench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 23 for the procedure. Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Assign Source Files dialog box is displayed. Select the structural VHDL netlist and testbench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the

Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

Note: SpeedWave can only simulate configurations. You must have at least one configuration in your testbench.

7. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double-click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.
8. **Simulate your design**. Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click Apply. Click Close when you have completed your simulation.

Timing Simulation (PC)

Use the following procedures to perform a timing simulation of an Actel design on a PC.

1. **Place-and-route your design in Designer.** Refer to the *Designer User's Guide* for information about using Designer.
2. **Extract timing information for your design from Designer.** From the File menu, click Export. Then, click Timing Files. Choose SDF and click Save (or click Back Annotate). The Back Annotate dialog box is displayed. Create a <design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Select your Actel project in Project Manager.** If you have not created a project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 15 for the procedure.
4. **Invoke SpeedWave.**
5. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click Cancel in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 16 for the procedure.

6. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select a .hws file and click Open in the Open dialog box.

7. **(Optional) Analyze your VHDL design files and testbench.** Skip this step if you are using the same structural VHDL netlist and testbench you analyzed for structural simulation. Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Assign the Add Source Files command from the Library menu. The Add Source Files dialog box is displayed. Select the structural VHDL netlist and testbench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your testbench.

8. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double-click “user.lib” and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

9. **Import the timing information for your design.** Click the VITAL Timing index tab. If you are running 7.4, click the Perform SDF Back Annotation check box. Then, click OK and the the Setup SDF Back Annotation dialog box is displayed. If you are running 7.5, do not click OK. Click the SDF Back Annotation tab at the top of the load VHDL Design window to open the Setup SDF Back Annotation dialog box. Type the name of your <design_name>.sdf in the SDF File box or use the Browse button.

10. **Add Scope options.** In the Scope window, fill in the name of the instance in the testbench you want to back annotate (e.g. “/uut”). Select the Delay Mode you want use (Minimum, Typical, or Maximum). Click Add and verify that the Scope, File, and Timing settings are correct in the main window. Use the Change and Remove buttons to make any corrections.

11. **Back annotate your design.** Click OK.

12. **Simulate the design**. Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click Apply. Click Close when you have completed your simulation.

Behavioral Simulation (UNIX)

Use the following procedure to perform a behavioral simulation of an Actel design on UNIX.

1. **Create a working directory.** For more information refer to the Innoveda manuals. Type the following command at the prompt:

```
vanlibcreate ./user.lib user
```

2. **Create a soft link to the Synopsys library.** Type:

```
ln -s $VANTAGE_VSS/pgm/libs/synopsys.lib synopsys
```

Note: When installing the Innoveda SpeedWave simulator, you have the option of installing a pristine IEEE library or the Synopsys version. You need the Synopsys library for compatibility with the Actel VITAL libraries. If you have installed the Synopsys version, you will need to include the Synopsys library in your invocations. This manual shows the commands for the Synopsys version of IEEE libraries.

3. **Analyze your vhdl design files and testbench.** Type:

```
analyze -src <behavioral>.vhd -lib user.lib -libieee -lib
synopsys
analyze -src <test_bench>.vhd -lib user.lib -libieee -lib
synopsys
```

4. **Map to the compiled Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, you must add the following switches when analyzing your VHDL design files:

```
analyze -src <behavioral>.vhd -lib user.lib -lib $ALSDIR/
lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
```

Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

```
library <vhd_fam>;
use <vhd_fam>.components.all;
```

5. **Simulate your design.** Type:

```
vbsim -cfg <configuration_name> -until complete -lib
user.lib -libieee -lib synopsys
```

6. **Map to the compiled Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, you must add the following switches when simulating your VHDL design files:

```
vbsim -cfg <configuration_name> -until complete -lib
user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/
swave/<vhd_fam>
```

In the above, <configuration_name> is the name of the configuration that binds the testbench entity and architecture.

For example:

```
vbsim -cfg test_add_behave -until complete -lib user.lib
-libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
```

Here the configuration named test_add_behave will be simulated.

Structural Simulation (UNIX)

Use the following procedure to perform a structural simulation of an Actel design on UNIX.

1. **Generate a structural VHDL netlist.**

If you are using Synopsys Design Compiler, generate the structural VHDL netlist from this tool.

If you are using other synthesis tools, generate a gate-level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a netlist using edn2vhdl,

type the following**:**

```
edn2vhdl FAM:{<act_fam>} [ EDNIN:<Edif_File1>[+<Edif_File2...>] ][ VHDOUT:<Vhdl_File> ]<design_name>
```

To generate a netlist using Designer Series software,

2. **Export a structural VHDL netlist.** From the File menu, choose Export, then Netlist. This displays the Export Netlist Files dialog box. In the Export Netlist Files dialog box, specify the File name and set the Save As type to VHDL. Click OK.

   Note: The VHDL generated by both Designer and the edn2vhdl program will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

3. **Analyze the structural VHDL and the testbench.** Type:

   ```
   analyze -src <structural>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys

   analyze -src <test_bench>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
   ```

4. **Perform a structural simulation of your design.** To perform a structural simulation using your SpeedWave simulator, type:

   ```
   vbsim -cfg <configuration_name> -until complete
   -lib user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/
   95/swave/<vhd_fam>
   ```

   For example:

   ```
   vbsim -cfg test_add_structure -until complete -lib user.lib
   -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
   ```

   Here the configuration specified by test_add_structure will be simulated.

Timing Simulation (UNIX)

Use the following procedure to perform a timing simulation of an Actel design on UNIX.

1. **Compile the structural netlist.** To perform a timing simulation using your SpeedWave simulator, compile your VHDL design and testbench files (if not already done for structural simulation) and run simulation.

   The following commands demonstrate how to compile VHDL design and testbench files:

   ```
   analyze -src <structural>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
   ```

   ```
   analyze -src <test_bench>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
   ```

2. **Run the backannotation simulation using the timing information from the SDF file.** Type:

   ```
   vbsim -cfg <configuration_name> -until complete -lib
   user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/
   swave/<vhd_fam> -sdf <design_name>.sdf <UUT> -sdfmode
   [min|typ|max]
   ```

   In the above, <configuration_name> is the name of your configuration that binds the testbench entity and architecture, <design_name> is name of the top-level entity, <UUT> is the instance of the top-level entity in the testbench.

7

Simulation with Synopsys VSS

This chapter describes steps to perform functional (behavioral and structural) and timing simulation for Actel devices using the Synopsys VSS simulator.

Behavioral Simulation

Use the following procedure to perform behavioral simulation.

1. **Create a working directory.** Type the following command at the prompt:

   ```
   mkdir work
   ```

2. **Using a text editor, create a ".synopsys_vss.setup" file in your current directory containing the following lines:**

   ```
   work > default
   default: ./work
   ```

3. **Map to the compiled Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, you must add the following line to your ".synopsys_vss.setup" file:

   ```
   <vhd_fam>: $ALSDIR/lib/vtl/95/vss/<vhd_fam>
   ```

4. **Analyze your VHDL design files and testbench.** Type the following command at the prompt:

   ```
   vhdlan <behavioral>.vhd
   vhdlan <test_bench>.vhd
   ```

5. **Create a vss.dofile to run simulation in batch mode.** Type the following command at the prompt:

   ```
   run
   quit
   ```

6. **Simulate your design.** Type the following command at the prompt:

   ```
   vhdlsim -t ps -i vss.dofile <configuration_name>
   ```

Structural Simulation

1. **Analyze your structural VHDL netlist and testbench.** If you have not already generated a structural netlist, go to "Generating a Structural VHDL Netlist" on page 23. Type the following command at the prompt:

```
vhdlan <structural>.vhd
vhdlan <test_bench>.vhd
```

2. **Simulate your design.** Type the following command at the prompt:

```
vhdlsim -t ps -i vss.dofile <configuration_name>
```

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place-and-route your design in Designer.** Refer to the *Designer User's Guide* for information about using Designer.
2. **Extract timing information for your design.** From the File menu, click Export. Then, click Timing Files. Choose SDF and click Save (or click Back Annotate). The Back Annotate dialog box is displayed. Create a <design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Analyze your structural VHDL netlist and testbench.** Type the following command at the prompt:

```
vhdlan <structural>.vhd
vhdlan <test_bench>.vhd
```

4. **Simulate your design using SDF back annotation.** Type the following command at the prompt:

   ```
   vhdlsim -t ps -i vss.dofile -sdf_max -sdf_top
   <top_entity_name>/<instance_name> -sdf <design_name>.sdf
   <configuration_name>
   ```

   Substitute "-sdf_min" or "-sdf_typ" for "-sdf_max" to use the minimum, typical delays, or maximum, respectively. Subsitute the name of your configuration that binds the testbench entity and architecture for <configuration_name>, the top-level entity in your testbench for <top_entity_name>, and the instance of the design for <instance_name>.

B

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1276 401500.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

(408) 522-4460
(800) 262-1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

Worldwide Sales Offices

Headquarters

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
Toll Free: 888.99.ACTEL

Tel: 408.739.1010
Fax: 408.739.1540

US Sales Offices

California

Bay Area
Tel: 408.328.2200
Fax: 408.328.2358

Irvine
Tel: 949.727.0470
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Index

A

Actel
  FPGA Libraries 16
  web site 50
  web-based technical support 50
Actel Manuals 7
Actel Project Setup 15, 17
  Project Manager 15
  SpeedWave 16
Actel VITAL Libraries
  Creating a swave Directory 12
Analyzing
  Test Bench 37, 38, 40
  VHDL Source File 37, 38, 40
Assumptions 6

B

Back Annotate 40
Behavioral Simulation 37
  Cadence Leapfrog Simulator 31
  Model Technology V-System Simulator 25
  SpeedWave 20, 37

C

Capturing a Design
  VHDL-Based 20
Configuration 38, 39, 40
Contacting Actel
  customer service 49
  electronic mail 50
  telephone 51
  toll-free 49
  web-based technical support 50
Conventions 6
  Document 6–??
Creating
  swave Directory 12
Customer service 49

D

Delay Mode 40
Design Creation/Verification 20
  Behavioral Simulation 20
  EDIF Netlist Generation 21
  Structural Simulation 21
  VHDL Source Entry 20
Design Flow
  Design Creation/Verification 20
  Design Implementation 21
  Programming 22
  Schematic-Based 22
Design Implementation 21
  Place-and-Route 21
  Timing Analysis 21
  Timing Simulation 22
Design Layout 21
  Model Technology V-System Simulator 29
Designer
  EDIF Option 23
  GENERIC Option 23
  Place-and-Route 21
  Software Installation Directory 6
  Structural Netlist Generation 23
  Timer Tool 21
  Timing Analysis 21
  VHDL Option 21, 23
  VIEWLOGIC Option 21
Device
  Programming 22
  Verification 22
Document Assumptions 6
Document Conventions 6, 6–??

E
- EDIF Netlist Generation 23
  - Synthesis-Based 21
- EDIF Option 23
- edn2vhdl 24, 27
- Electronic mail 50, 51

F
- FPGA Libraries 16

G
- Generating
  - EDIF Netlist 21, 23
  - Structural Netlist 23
- Generating an EDIF netlist
  - Model Technology V-System Simulator 27
  - Viewlogic Vantage Speedwave Simulator 43
- GENERIC Option 23

I
- Importing Timing Information 40

L
- Libraries
  - Actel FPGA 16
  - Project 16

N
- Netlist Generation
  - EDIF 21

O
- Online Help 7

P
- Place-and-Route 21
- Postsynthesis Simulation 22
- Primary Directory 15
- Product support 49–52
  - customer service 49
  - electronic mail 50, 51
  - oll-free line 49
  - technical support 50
  - web site 50
- Programming a Device 22
- Project Manager
  - Project Setup 15
  - Selecting an Actel FPGA Library 16
  - Setting the Primary Directory 15
- Project Setup 17
  - Project Manager 15
  - SpeedWave 16

S
- Schematic-Based Design Flow 22
- Scope Options 40
- Selecting an Actel FPGA LIbrary 16
- Selecting Scope Options 40
- Setting the Primary Directory 15
- Setting Up
  - an Actel Project in Project Manager 15
  - an Actel Project in SpeedWave 16
- Setup Procedure
  - Cadence Leapfrog Simulator (VITAL 95) 12
- Setup Procedures 17
  - Creating a Project Library 16
  - Project Setup 17
  - Setting Up an Actel Project 15
  - User Setup 13
- Simulation

  - Behavioral 20
    - SpeedWave
      - Behavioral Simulation 37
  - Configuration 38, 39, 40
  - Postsynthesis 22
  - SpeedWave 20, 21, 22
  - Structural 21, 38
  - Synthesis-Based 20, 21, 22
  - Synthesis-Based Simulation
    - SpeedWave 37
  - Test Bench 38, 39, 40
  - Timing 22
- SpeedWave
  - Behavioral Simulation 20
  - Creating a Project Library 16
  - Importing Timing Information 40
  - Postsynthesis Simulation 22
  - Scope Options 40
  - Structural Simulation 21, 38
  - Timing Simulation 22
- Static-Timing Analysis 21
- Structural Netlist Generation
  - Designer 23
  - EDIF Option 23
  - edn2vhdl 24, 27
  - GENERIC Option 23
- Structural Simulation 21, 38
  - Cadence Leapfrog Simulator 32
  - Model Technology V-System Simulator 27
  - SpeedWave 21, 38
  - Viewlogic Vantage Speedwave Simulator 42
- swave Directory 12
- System Verification 22
  - Silicon Explorer 22

T

- Test Bench 37, 38, 40
  - Modifying 21
- Timer, Static-Timing Analysis 21
- Timing Analysis 21
- Timing Information 40
- Timing Simulation 22
  - SpeedWave 22
- Toll-free line 49

U

- Unit Delays 20
- User Setup 13

V

- Verilog Design Flow
  - Programming 22
- VHDL
  - Option 23
- VHDL Option 21
- VHDL Source Entry 20
- VHDL Source File
  - Analyzing 37, 38, 40
- VHDL Synthesis-Based Design Flow
  - Design Creation/Verification 20
  - Design Implementation 21
- VIEWLOGIC Option 21

W

- Web-based technical support 50