LC Tank Voltage Controlled Oscillator Tutorial

by

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Introduction by

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Abstract

This tutorial provides an introduction to the fundamentals of LC tank voltage controlled oscillator analysis and design.

Acknowledgments

I would like to thank Professor John Starr Jamel for allowing the UW ASIC Analog Group to utilize his tutorial within the UW ASIC Analog Group.

Dedication

This tutorial is dedicated to the students of the UW ASIC Analog Group.

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Chapter 1

Introduction

The Analog Group, of the UW ASIC Group, has decided to concurrently design two different VCO (Voltage Controlled Oscillator) topologies. This introduction provides some of the reasoning for why the Analog Group has chosen to design VCOs that have the ring oscillator and the LC tank topology.

There are two types of VCOs that one may choose to design:

1) waveform oscillators

2) resonant oscillators.

Waveform oscillators:

1) ring oscillator topology

2) relaxation oscillator (which has poor phase noise performance).

Resonant oscillators:

1) LC tank oscillator topology

2) crystal oscillator (which is neither integrated nor tunable).

Ideally a given VCO topology would be able to meet all of the specifications listed in Table 1.1.

Table 1.1: List of ideal VCO specifications.

1) low noise
2) low power
3) integrated
4) wide tuning range
5) small die area occupancy
6) high frequency (GHz)

As discussed below, it is unlikely that either the ringVCO (ring oscillator VCO) or LCVCO (LC tank VCO) topologies can meet all of these specifications.

Through a comparison of ringVCOs and LCVCOs, the following advantages and disadvantages may be formulated.

RingVCO advantages:

1) highly integrated in VLSI

2) low power

3) small die area occupancy

4) wide tuning range.

RingVCO disadvantages:

1) As frequency increases phase noise and jitter performance degrades.

LCVCO advantages:

1) outstanding phase noise and jitter performance at high frequency.

LCVCO disadvantages:

1) contains an inductor and a varactor (variable capacitor) which are large area components, and thus is not as suitable for VLSI

2) high power consumption

3) occupies a large die area

4) small tuning range.

Clearly, the ringVCO is most suitable for low power, highly integrated applications that require a large tuning range and a low die space area. In contrast, the LCVCO out performs the ringVCO in low noise applications.

For mobile wireless applications one desires low power, hence the ringVCO may be of choice. However, wireless applications require outstanding noise (phase noise and jitter) performance at high frequency, hence the LCVCO may be of choice.

Having said that, there may be specific applications where either the ringVCO or the LCVCO topology may be optimized to perform sufficiently well.

The aforementioned advantages and disadvantages should hold true for the fabrication technologies (0.13μm CMOS, etc) that are predicted, by IRTS road map, to be in use in the future. Hence, a design decision - to utilize either a ringVCO or a LCVCO - that is based on the above advantages and disadvantages should be a valid decision in the future when silicon CMOS fabrication technologies scale further into the deep deep sub-micron regime.

This analysis illustrates that to be able to target the most diverse range of applications, one should be knowledgeable in the design and optimization of both the ringVCO and LCVCO topologies.

The forthcoming tutorial provides fundamental information on the analysis and design of a LCVCO.

Ryan Norris,

2005 UW ASIC Analog Group leader

Chapter 2

LC Tank Voltage Controlled Oscillator Tutorial

Please see the Section entitled Bibliography at the end of this document for a list of useful references [1] [2] [3] [4].

2.1 Voltage Controlled Oscillator Analysis and Design

An LC tank VCO can be thought of as two 1-port networks connected together.

Figure 2.1: LC Tank.

One 1-port represents the frequency selective "tank" where the oscillations occur and the other 1-port represents the active circuit that cancels the losses in the tank.

Oscillations can occur when:

i) the negative conductance of the active network cancels out the positive conductance (loss) of the tank

ii) the closed loop gain has zero phase shift.

Conditions i) & ii) above amount to a closed loop gain greater than or equal to unity magnitude with no imaginary component.

The first step in designing an oscillator is to choose a circuit topology or type.

For this example a balanced NMOS VCO will be chosen.

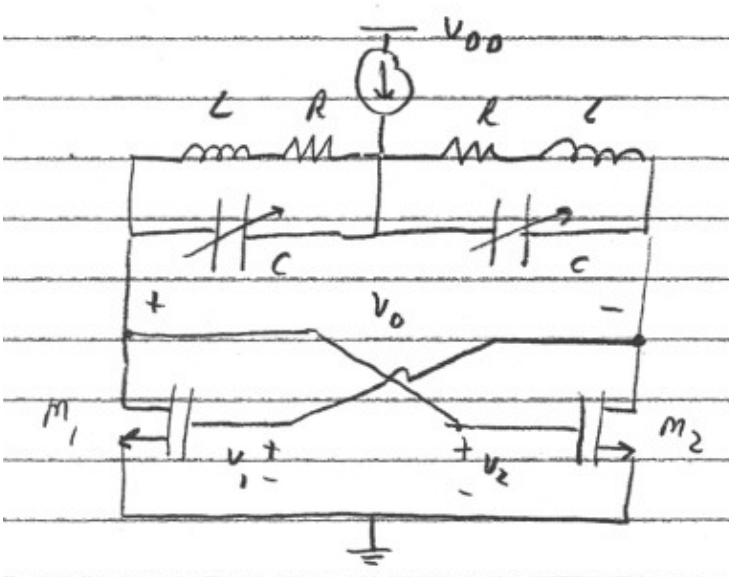


Figure 2.2: Balanced NMOS VCO.

The only losses being assumed in Figure 2.2 are those associated with the inductor. In reality there would also be losses associated with the variable capacitors (varactors) and the MOSFETs (the active devices).

In practical integrated VCOs the inductors are on-chip spiral inductors with low quality factor that dominates the losses of the VCO tank.

The quality factor Q_L of the inductor is given by

$$Q_L = \frac{\omega_o L}{R} \tag{2.1}$$

where

ω_o is the oscillation frequency [rad/s]

L is the value of the inductance [H]

R is inductor's equivalent series resistance [Ω].

Q_L in practical silicon RF IC processes ranges from 5 to 10.

Values of on-chip inductances range from 0.1 nH to 10 mH in practical RF IC processes.

It can be shown that the oscillation frequency of the circuit shown in Figure 2.1, assuming ideal varactors and MOSFETs is given by

$$\omega_o = \frac{1}{\sqrt[2]{LC}} \sqrt[2]{1 - \frac{R^2 C}{L}} \tag{2.2}$$

It can also be shown, under the same set of assumptions that the g_m of each MOSFET must be

$$g_m \geq \frac{RC}{L} \tag{2.3}$$

for oscillation to occur.

2.1.1 Small Signal (a.c.) Analysis

The oscillator is essentially a differential pair that have been cross-coupled in a positive feed back configuration.

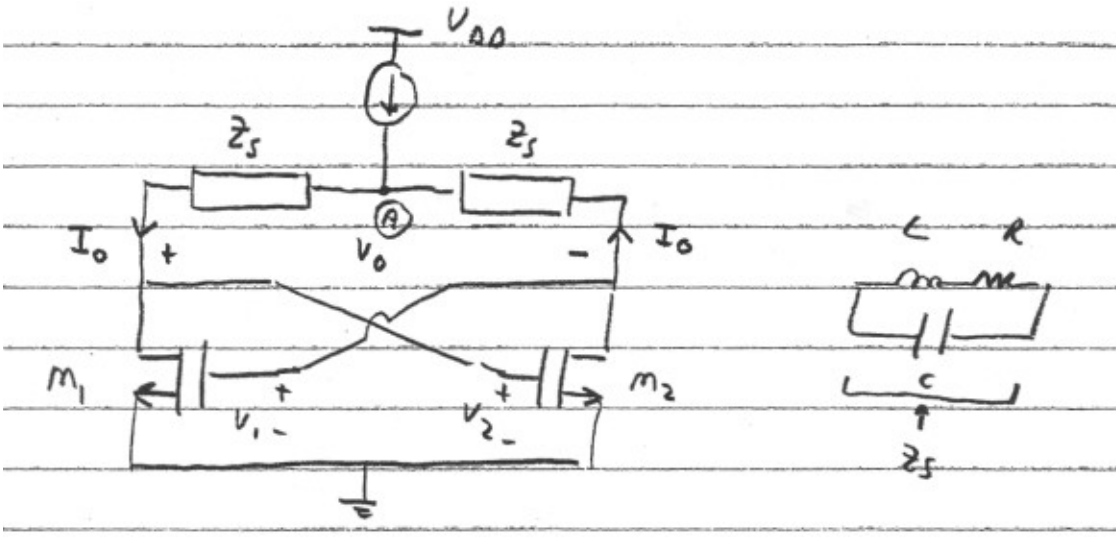


Figure 2.3: Balanced NMOS VCO with each tank represented by a series impedance.

The input of each transistor in the differential pair has been connected to the output of the opposite transistor.

The output voltage $v_o = v_1 - v_2$ is a differential output signal.

v_1 which is the input signal to M_1 is also the single ended output of M_2.

Each individual transistor in the pair is essentially a common-source amplifier with a complex, tuned load comprised of a lossy inductor in parallel with a capacitor.

The Z_s load is called a "tank" circuit since it holds the oscillating energy like a tank at the oscillation frequency.

The two separate tanks form a differential load to the differential pair where node 'A' remains, to first order, at the same potential during oscillations.

Node 'A' is a "virtual" a.c. ground point in the same manner as the virtual ground that exists in a normal differential amplifier.

Node 'A' is not a complete a.c. short, however, since, ideally, there should be an infinite a.c. impedance between this node and the power supply rail V_{DD}.

A proper active current source must be designed to provide the d.c. biasing to node 'A' and hence M_1 and M_2 as well as maintaining a high a.c. impedance between node 'A' and the supply rail.

If the a.c. impedance between node 'A' and V_{DD} is not high, then RF energy will "leak" out of the tanks into the supply rail destroying the oscillations.

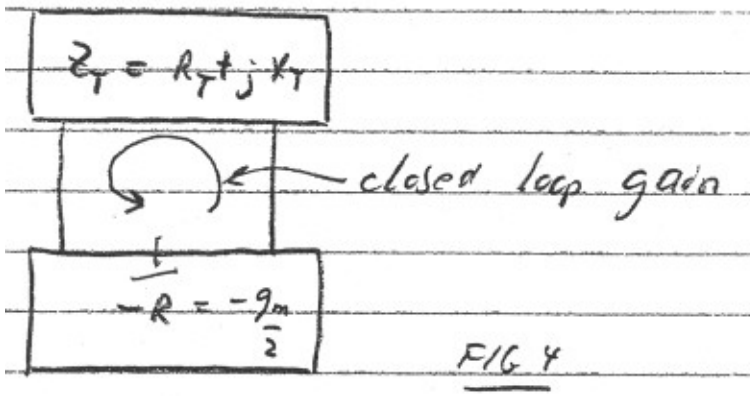


Figure 2.4: VCO of Figure 2.3.

For small signal (a.c.) analysis the current source of Figure 2.3 behaves as an open circuit. The VCO of Figure 2.3 can then be represented by Figure 2.4 as two 1-port networks. Assuming ideal MOSFETs (i.e. no parasitic resistances or capacitances), the entire differential amplifier can be modeled as a negative resistance $-R$ (or negative conductance $-G_m = -\frac{g_m}{2}$).

The two tank circuits appear in series where

$$Z_T = 2Z_s = R_T + jX_T = 2(R_s + jX_s) \tag{2.4}$$

The oscillation condition requires that the closed loop gain (around the two 1-ports) be of at least unity magnitude and zero phase angle. The zero closed loop phase condition implies that at the frequency of oscillation, ω_o, $X_T(\omega_o) = 0$.

The magnitude of the amplifier negative resistance must be at least as large as $R_T(\omega_o)$, the total resistive or real loss of the two tanks.

$\therefore$ setting $X_T(\omega_o) = 0$ determines ω_o and setting $|-\frac{1}{R}| = |-\frac{g_m}{2}| = \frac{1}{R_T(\omega_o)}$ determines the minimum g_m of each MOSFET for oscillation to occur.

In general, the negative resistance of the differential pair must overcome all real resistive losses in the oscillator circuit. An ideal oscillator has no losses with infinite voltage swing at precisely one frequency.

The presence of losses results in a finite voltage swing over a narrow spread of frequencies.

How ideal an oscillator is can be directly related to the "quality factor" of the tank.

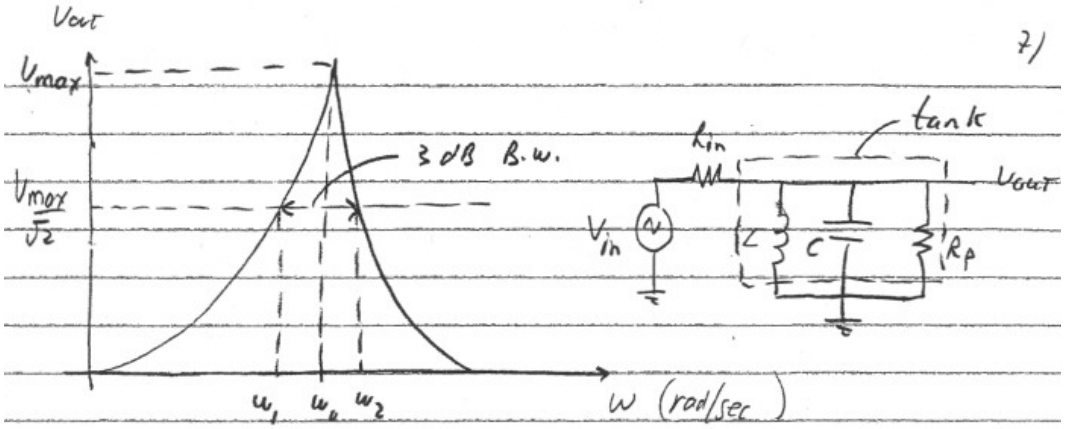


Figure 2.5: Bandwidth of an LC tank oscillator.

At resonance, a pure LC tank with no losses presents infinite impedance to an applied signal across the tank. This implies that the output voltage across the tank will be infinite if the tank is driven by a source with infinite impedance.

If the tank has real losses, however, even if it is driven by an infinite impedance source (i.e. $R_{in} = 0$), the losses can be modeled as if the lossless tank had a finite impedance load, $R_p \neq \infty$.

The finite impedance load R_p will "de-Q" the tank resulting in a finite output voltage.

One definition of quality factor or "Q" is

$$Q = \frac{\omega_o}{\omega_1 \omega_2} \tag{2.5}$$

as per Figure 2.5.

It can be shown that Equation 2.5 is also equal to

$$Q_{loaded} = \frac{R_p}{\omega_o L} \tag{2.6}$$

where ω_o is the resonant frequency of the lossless tank

$$w_o = \frac{1}{\sqrt[2]{LC}} \tag{2.7}$$

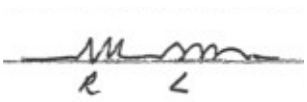
Equation 2.6 is known as a "loaded Q".

The "loaded Q" can be related to something called a "component Q" where the parallel resistance, R_p, modeling the total losses of the tank can be related to the individual losses of the inductor and capacitor components themselves.

The component Q of the inductor is given by

$$Q_L = \frac{\omega_o L}{R} \tag{2.8}$$

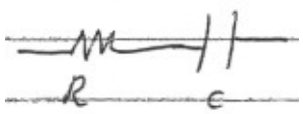
where R is the series resistance of the inductor.



The component Q of the capacitor is given by

$$Q_C = \frac{1}{R\omega_o C} \tag{2.9}$$

where R is the series resistance of the capacitor.



The total loaded Q can then be estimated as

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_L} + \frac{1}{Q_C}. \tag{2.10}$$

Often capacitors have much higher component Q's than inductors in silicon integrated processes (though this may not be the case if varactors are used as the capacitor) such that

$$Q_L << Q_C \tag{2.11}$$

Then $Q_L \approx Q_{loaded}$.

One can then write $Q_{loaded} = \frac{R_p}{\omega_o L} = Q_L = \frac{\omega_o L}{R} = Q$ as the quality factor of the lossy tank.

$$\implies R_p = \frac{(\omega_o L)^2}{R} = (\frac{\omega_o L}{R})^2 R = Q^2 R \tag{2.12}$$

where R is the series resistance of the inductor, R_p is the equivalent parallel resistance of the lossy tank, and Q is the quality factor of the lossy tank $\equiv$ the component Q of the inductor $\equiv$ the loaded Q of the lossy tank (under the assumption made thus far).

From Equation 2.12, the total finite a.c. impedance shunting an otherwise perfect LC tank can be related to the series resistance of the inductor and the component Q of the inductor.

It is desirable to have as large of an R_p as possible for a good oscillator.

In practice, an RF IC designer sets the value of L required for an oscillator, and then attempts to layout the inductor for maximum component Q so that R_p is as high as possible.

Generally over a reasonable range of on-chip inductors the maximum Q possible is more or less independent of the value of inductance provided the particular inductor layout is optimized for maximum Q given the technology being used.

Also, the maximum Q is more or less independent of frequency over a fairly large frequency range since inductor layout can also be optimized for different frequencies of operation.

For the above reasons, one usually attempts to determine the maximum reasonable Q one can expect over a range of inductance values and frequency ranges for a given technology. Then this value is used as a constant in the initial design process.

Typical values of Q that can be obtained in today's deep sub-micron processes (silicon CMOS) for on-chip inductors range from 5 to 10 for inductor values ranging from 0.1 to 10 nH and frequencies ranging from 1 to several GHz.

2.1.2 Design Constraints

VCOs are generally designed for minimum phase noise under constraints of d.c. power dissipation, tuning range, output voltage swing and die area.

Usually on-chip spiral inductors are utilized for this type of VCO. These inductors usually dominate the chip area required ranging in diameter from 100 to 500 μm.

The d.c. power dissipation is given by

$$V_{supply} I_{bias} \leq P_{dissipation\_max} \tag{2.13}$$

The magnitude of the output voltage at the drains of the NMOS transistors is governed, to first order, by the a.c. impedance of the lossy tank: $V_{tank} \approx I_{bias} R_p$ where $R_p = Q_L \omega_o L$ and V_{tank} is the single-ended peak-to-peak voltage swing at either the + or - output node of the VCO before any output buffering.

The tuning range of a VCO is required to be in excess of a certain minimum percentage of the center frequency, ω_o. The LC tank is made tunable by implementing the 'C' of the LC tank using a varactor (variable capacitor). The varactor is designed to be adjustable over some range C_{tank_min} to C_{tank_max}.

Assuming that $\omega_o \approx \frac{1}{\sqrt[2]{LC}}$ (i.e. that of an ideal tank) then,

$$L_{tank} C_{tank\_min} = \frac{1}{(\omega_{max})^2}; L_{tank} C_{tank\_max} = \frac{1}{(\omega_{min})^2} \tag{2.14}$$

where $(\omega_{max} - \omega_{min})/\omega_o$ = fractional tuning range and $(\omega_{max} + \omega_{min})/2 = \omega_o$

The minimum criterion for oscillation is that the closed loop gain, α, is at least unity. In practise designers set the g_m of the NMOS transistors so that α exceeds the absolute minimum value of 1 such that the minimum designed α becomes $\alpha_{min} > 1$.

An α_{min} of 2 or 3 is often used.

Finally, assuming that the on-chip spiral inductors are limiting chip-area one usually determines the inductor diameter d such that it is $\leq$ some maximum possible value ($d \leq d_{max}$).

2.1.3 Transistor Non-Idealities

MOSFETs have many parasitic capacitances and resistances that determine transistor performance.

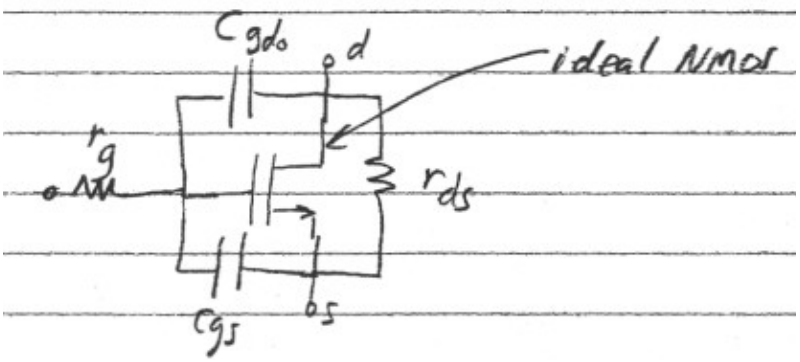


Figure 2.6: MOSFET parasitic elements.

Parasitic resistances increase the losses in the VCO requiring a higher g_m compared to the ideal transistor case.

Parasitic capacitances can combine with the tank capacitance, C, reducing the oscillation frequency. Therefore the tank's C must be decreased to allow for these parasitic transistor capacitances.

Parasitic resistances will also contribute thermal noise increasing oscillator phase noise.

r_{ds} is not a real resistance contributing noise, but results from channel path length modulation decreasing the a.c. output resistance of the MOSFET and partially de-Q's the LC tank.

As shown in Figure 2.7 a) and b), ignoring the effects of gate resistance r_g, it can be shown that r_{ds} appears in parallel with R_p if node 'A' can be assumed to experience no a.c. voltage fluctuations during oscillation (i.e. node 'A' is a virtual ground).

All parasitics can be associated with the tank as shown in Figure 2.7 leaving ideal NMOS transistors in the active 1-port circuit.

The oscillation frequency ω_o will them be altered such that

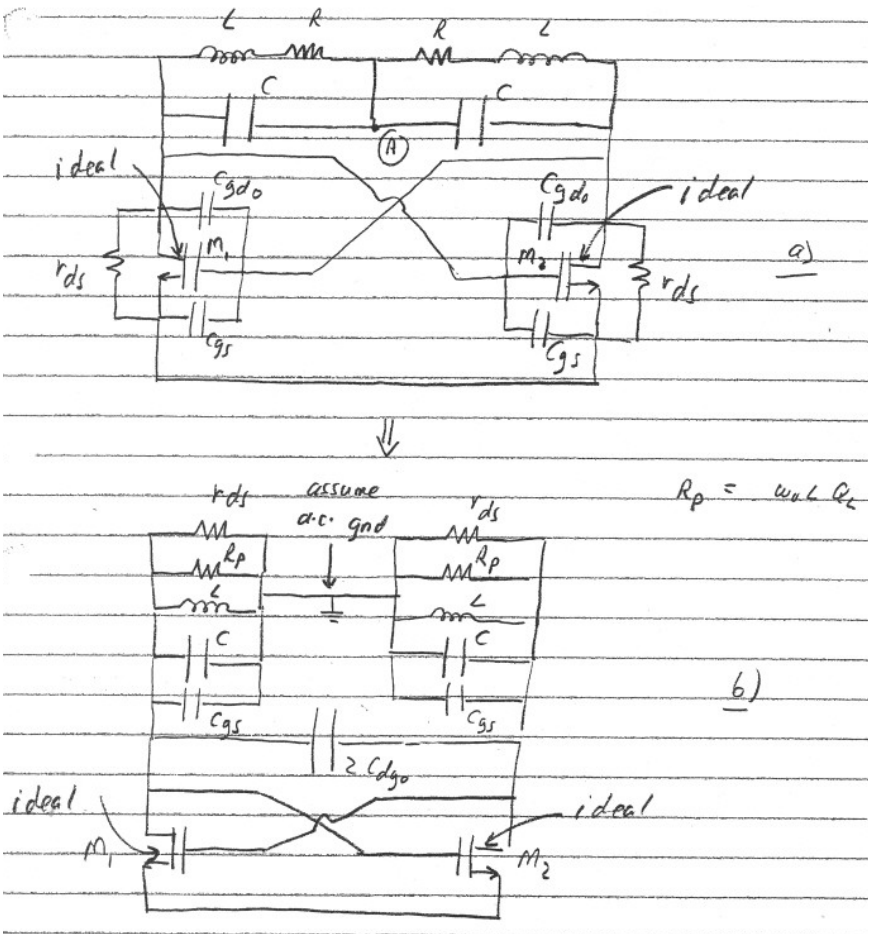


Figure 2.7: LC tank parasitic elements.

$$\omega_o = \frac{1}{\sqrt[2]{L(C + C_{gs} + 4C_{gd_o})}} \sqrt[2]{1 - \frac{R^2(C + C_{gs} + 4C_{gd_o})}{L}} \tag{2.15}$$

In the above equation it can be seen that the transistor capacitances more or less simply add to the tank capacitance, C, requiring a decrease in C compared to the ideal case for a given ω_o.

The start-up g_m condition also changes such that the absolute minimum g_m required for oscillation becomes:

$$g_m \geq \frac{1}{r_{ds}} + \frac{R(C + C_{gs} + 4C_{gd_o})}{L} \tag{2.16}$$

Equation 2.16 states the important result that the bigger the MOSFETs the higher the g_m must be to achieve oscillation.

2.1.4 Determining Transistor Width 'W'

The NMOS transistors must be biased and laid out such that the required g_m is obtained to overcome all losses including those of the tank and the transistors themselves.

The above amounts to determining the V_{gs} (the bias) and W for a given minimum transistor channel length $L_{channel}$, which is fixed for a given process technology.

For modern CMOS processes V_{gs} is selected such that $V_{gs} - V_t \approx 0.4$ to 0.5, where V_t is the MOSFET threshold voltage. If $V_{gs} - V_t$ is too high, g_m is degraded due to effects such as mobility degradation and saturate velocity effects for channel carriers. If $V_{gs} - V_t$ is too small then W must be very large such that the transistor will not fit into the require area, or such that g_m is always too large according to Equation 2.16 too obtain.

To estimate the required g_m one must iterate on device equations for I_d, g_m, r_{ds}, C_{gs}, C_{gd_o} and the equation for start-up criterion of Equation 2.16. Assume the MOSFETs are in saturation.

A basic Level 1 MOS model gives:

$$I_{dsat} = \frac{k_p}{2}\frac{W}{L_{channel}}(V_{gs} - V_t)^2 = \frac{g_m}{2}(V_{gs} - V_t) \tag{2.17}$$

$$g_m = \frac{dI_{dsat}}{dV_{gs}} = k_p\frac{W}{L_{channel}}(V_{gs} - V_t) \tag{2.18}$$

$$r_{ds} = \frac{1}{\lambda I_{dsat}} \tag{2.19}$$

$$C_{gs} = \frac{2}{3} C_{ox} W L_{channel}; C_{gd_o} = C_{GD_o} W \tag{2.20}$$

Certain model parameters must be determined from the design kit for the CMOS process including:

$L_{channel}$ = min channel length

V_t = threshold voltage

k_p

λ - models channel length modulation

$C_{ox} = t_{ox}/\epsilon_{ox}$, t_{ox} = gate oxide thickness

G_{GD_o} = gate-to-drain capacitance per unit gate width W.

Some of the model parameters must be determined for a combination of other parameters.

Begin the iteration process assuming ideal MOSFETs and including only the tank losses due to R.

$$\therefore g_m = \frac{RC}{L} \tag{2.21}$$

(once C and L are known - see design procedure steps)

from Equation 2.18 we have

$$W = \frac{g_m L_{channel}}{k_p (V_{gs} - V_t)} \tag{2.22}$$

then calculate I_{dsat}, r_{ds}, C_{gs}, C_{gd_o} from Equations 2.17 to 2.20.

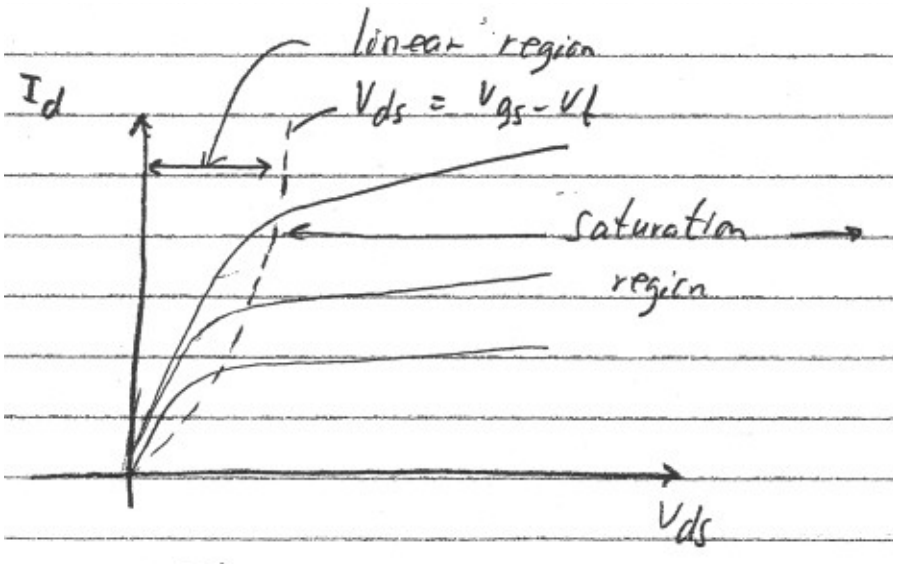


Figure 2.8: MOSFET I-V characteristics.

I_{dsat} is the drain current under saturation conditions.

A higher g_m will be required for non-ideal case using

$$g_m = \frac{1}{r_{ds}} + \frac{R(C + C_{gs} + 4C_{gd_o})}{L} \tag{2.23}$$

W is then increased according to Equation 2.22, etc. until convergence is obtained.

Tank C can then be adjusted to obtain the require ω_o from Equation 2.15 once final values of C_{gs}, C_{gd_o}, etc., are known.

The above method is only approximate and W and g_m will have to be adjusted once realistic higher level NMOS models are used (i.e. BSIM3) and transistor layout is completed since actual layout will affect C_{gs} and G_{gd_o}.

The above assumes that one will use a very wide single stripe MOSFET. In reality multiple finger MOSFETs are used to obtain a total W to reduce series gate resistance and to provide a more compact layout with lower parasitic capacitances.

Actual g_m should be above the minimum estimated using Equation 2.23 by some safety factor α_{min} (e.g. 2 or 3). Therefore, incorporate this safety factor into the iteration from the beginning.

2.1.5 VCO Design Procedure

Certain design specifications must be given:

a) max d.c. power dissipation = $V_{supply}I_{bias}$

b) min output voltage swing (single-ended) = V_{tank}

c) tuning range in percentage = $\frac{\omega_{max}-\omega_{min}}{\omega_o} \times 100\%$

d) $\alpha_{min} > 1$

e) chip area

f) Frequency of operation (ω_o)

The goal of the design is then to develop a VCO that meets the above constraints with minimum phase noise.

An alternative strategy may be to design a VCO with a pre-specified phase noise but where the d.c. power dissipation is minimized.

Design Procedure Steps

1) Set $I_{bias} = \frac{P_{d.c.\_max}}{V_{supply}}$

2) Determine max Q_L of inductors for a given process at required frequency ω_o. This can be determined in may ways including

i) already known from previous design experience in that particular process

ii) read from model elements in design kit

iii) determined through exhaustive design and optimization of inductor using electromagnetic simulation packages

iv) measured data taken from test inductors already fabricated in the same process.

3) Using $V_{tank} = I_{bias}R_p = I_{bias}\omega_o L Q_L$, set L so that V_{tank} is at the minimum required voltage swing for the design. I_{bias}, ω_o and Q_L area already known.

Caution: values of L must be chosen such that it is in a practical value range to be fabricated as well as being at a value that results in a practical value of capacitance, C, for the varactor.

4) Using $\omega_o = \frac{1}{\sqrt[2]{LC}}\sqrt[2]{1 - \frac{R^2C}{L}}$ where $R = \frac{\omega_o L}{Q_L}$ = effective series resistance of inductor, calculate the required value of C for the LC tank with ω_o being the center frequency of the VCO.

5) Given the minimum closed loop gain $\alpha_{min} > 1$ calculate the minimum transconductance of each NMOS transistor g_m such that $g_m = \alpha_{min}\frac{RC}{L}$

6) Take transistor non-idealities into account to arrive at a new g_m and also a transistor width, W, *as per Prof. Hamel's E&CE 439 lecture notes*.

2.2 Oscillator Phase Noise

Noise is injected into an oscillator by the devices that constitute the oscillator itself including the active transistors and passive elements.

This noise will disturb both the amplitude and frequency of oscillation.

Amplitude noise is usually unimportant because non-linearities that limit the amplitude of oscillation also stabilize the amplitude noise.

Phase noise, on the other hand, is essentially a random deviation in frequency which can also be viewed as a random variation in the zero crossing points of the time-dependent oscillator waveform.

Let $\gamma(t) = Acos\lfloor\omega_o t + \phi_n(t)\rfloor$ where A is the noiseless oscillator amplitude, ω_o is the oscillator frequency, $\phi_n(t)$ is the phase noise, $\gamma(t)$ is the oscillator output signal.

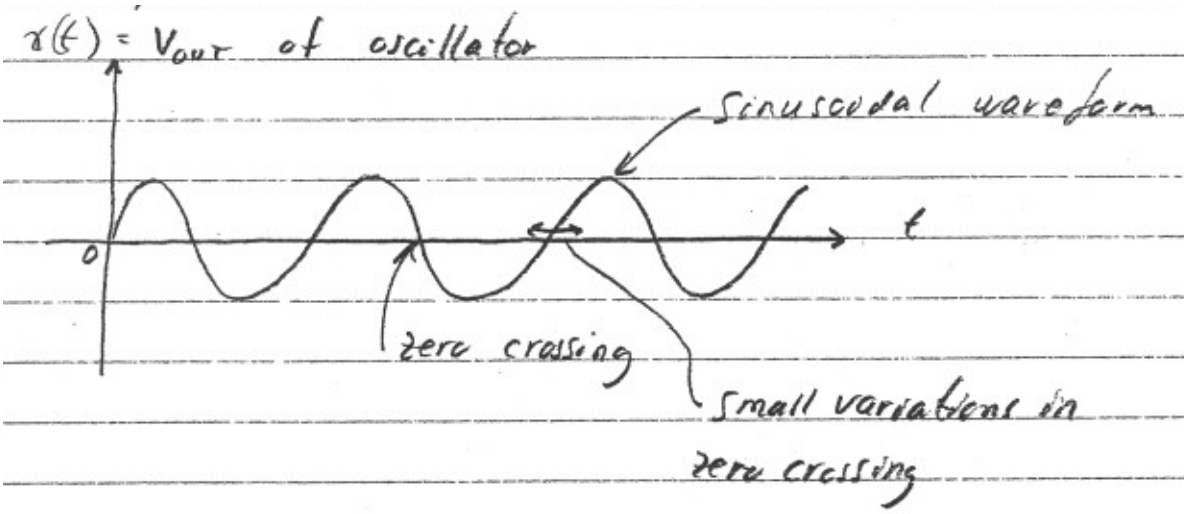


Figure 2.9: Illustration of phase noise in the time domain.

For Small $\phi_n(t)$

$\gamma(t) = Acos\lfloor\omega_o t + \phi_n(t)\rfloor$

$= A\lfloor cos(\omega_o t)cos(\phi_n(t)) - sin(\omega_o t)sin(\phi_n(t))\rfloor$

$\approx Acos(\omega_o t) - A\phi_n(t)sin(\omega_o t)$

since $cos(\phi_n(t)) \approx cos(0) = 1$ and $sin(\phi_n(t)) \approx \phi_n(t)$ for small $\phi_n(t)$

$\therefore$ the spectrum of the noise noise $\phi_n(t)$ is effectively translated to the oscillation frequency ω_o

i.e. the phase noise signal is amplitude modulating a sinusoid signal of frequency ω_o that is in turn superimposed on the ideal oscillator itself.

An oscillator, however, is a frequency selective (or narrow band, high quality factor) circuit and will tend to reject out of band (i.e. frequencies offset from ω_o) signals to some degree. This rejection increases at larger offsets from ω_o.

As a result, the effect of the noise sources is to produce "skirts" on either side of the ideal impulse function of the oscillator in the frequency domain.

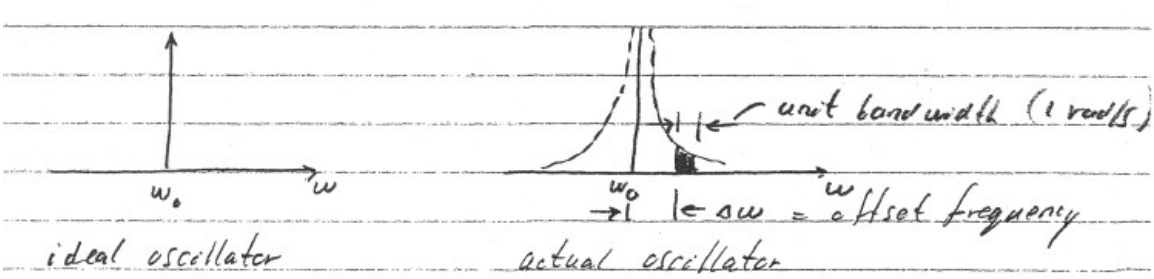


Figure 2.10: Illustration of phase noise in the frequency domain.

To measure or quantify phase noise, one considers a unit bandwidth at an offset $\Delta\omega$ with respect to ω_o, calculates the noise power in this bandwidth, and divide the result by the average carrier power.

e.g. carrier power = -2dBm, noise power measured in a 1kHz bandwidth at an offset of 1MHz = -70 dBm

0 dBm

= 1 mW of power,

dBm

$= 10\log_{10}(\frac{Power\_in\_watts}{10^{-3}watts})$

$= 10\log_{10}(Power\_in\_mW)$

$\therefore$ -70dBm $= 10\log_{10}(Power\_in\_mW)) \implies = -70dBm \Leftrightarrow P = 10^{-7}mW = 10^{-10}W$

$\therefore$ noise power in 1Hz bandwidth $= \frac{10^{-7}}{10^3} = 10^{-10}mW/Hz \Leftrightarrow 10log_{10}(10^{-10}) = -100dBm$

Dividing by carrier power amounts to adding 2dBm

$\therefore$ phase noise = -100 - (-2) = -98 dBc/Hz

dBc means "in dB with respect to carrier power."

2.2.1 Quality Factor 'Q' of an Oscillator

Phase noise of an LC oscillator depends on the Q of the LC tank circuit.

For an LC tank, Q is an indication of how much of the energy is lost as it is transferred from the capacitor to the inductor and vice versa.

Three Definitions of Q

1) One definition of Q defines it as:
$2\pi \frac{energy\_stored}{energy\_dissipated}$ per cycle

2) Q can also be defined as the "sharpness" of the magnitude of the frequency response

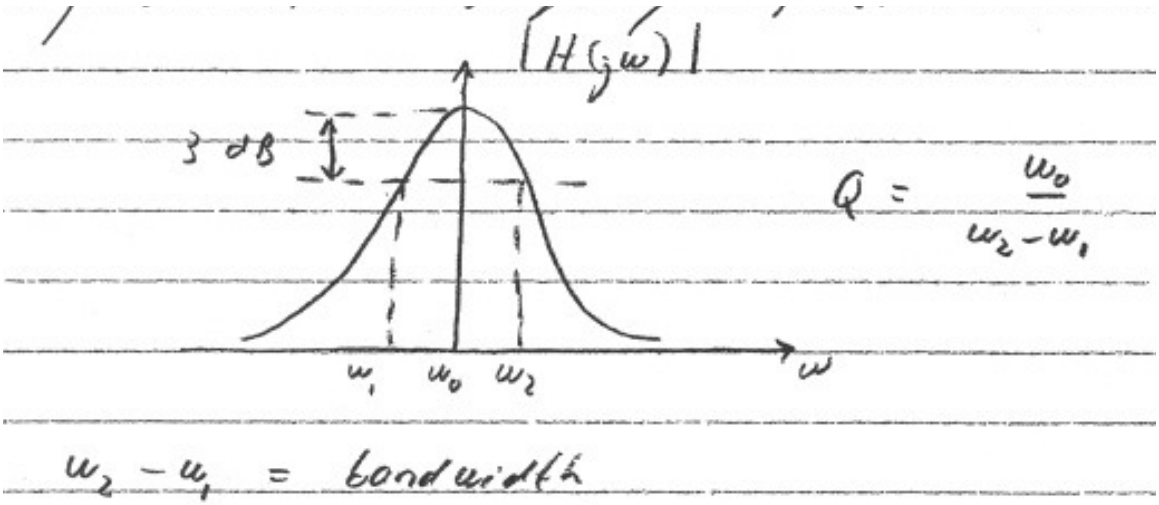


Figure 2.11: Calculation of Q from the frequency response.

3) Q can also be defined with respect to the phase of the open-loop transfer function $\phi(\omega)$ at the resonance of the LC tank in an oscillator

$Q = \frac{\omega_o}{2} |\frac{d\phi(\omega)}{d\omega}|$ at $\omega = \omega_o$

where ω_o = resonant frequency

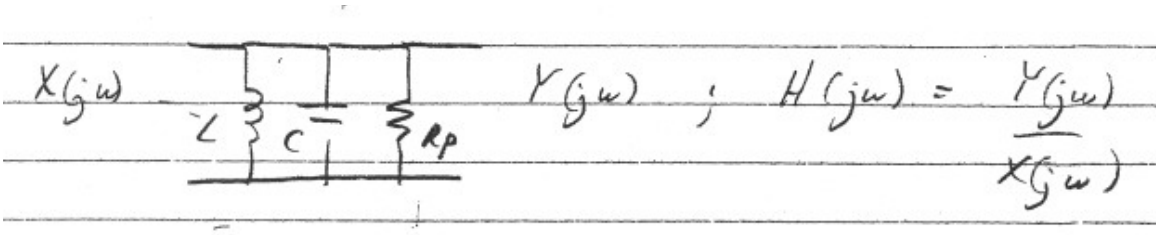


Figure 2.12: LC tank VCO open-loop transfer function.

$H(j\omega) = Z(j\omega) =$ open-loop transfer function

$\phi(j\omega) = tan^{-1}(\frac{Imag(Z(j\omega))}{Real(Z(j\omega))})$

$\frac{1}{Z} = j\omega C + \frac{1}{j\omega L} + \frac{1}{R_p} = j(\omega C - \frac{1}{\omega L}) + \frac{1}{R_p}$

$Z = \frac{1}{j(\omega C - \frac{1}{\omega L}) + \frac{1}{R_p}} = \frac{j(\frac{1}{\omega L} - \omega C) + \frac{1}{R_p}}{((\omega C - \frac{1}{\omega L}))^2 + (\frac{1}{R_p})^2}$

$\phi(j\omega) = tan^{-1}(\frac{\frac{1}{\omega L} - \omega C}{\frac{1}{R_p}}) = tan^{-1}(\frac{R_p(1-\omega^2 LC)}{\omega L}) = tan^{-1}[R_p(\omega L)^{-1}(1 - \omega^2 LC)]$

use $\frac{d(tan^{-1}u)}{dx} = \frac{1}{1+u^2}\frac{du}{dx}$

$\therefore \frac{d\phi}{d\omega} = \frac{1}{1+(\frac{R_p}{\omega L}(1-\omega^2 LC))^2}[\frac{-R_p}{(\omega L)^2}(1 - \omega^2 LC) - 2\frac{\omega LC}{\omega L}R_p]$

$\omega_o = \frac{1}{\sqrt[2]{LC}} \therefore 1 - \omega_o^2 LC = 0$

$\therefore \frac{d\phi}{d\omega}|_{\omega=\omega_o} = -2CR_p$

$\frac{\omega_o}{2}|\frac{d\phi}{d\omega}|_{\omega=\omega_o} = \omega_o CR_p = \frac{R_p}{X_C}$ where $X_C = \frac{1}{\omega_o C}$

at resonance $X_L = X_C$ where $X_L = \omega_o L$

$\therefore$ $\boxed{Q = \frac{\omega_o}{2}|\frac{d\phi}{d\omega}|_{\omega=\omega_o} = \omega_o CR_p = \frac{R_p}{\omega_o L}}$

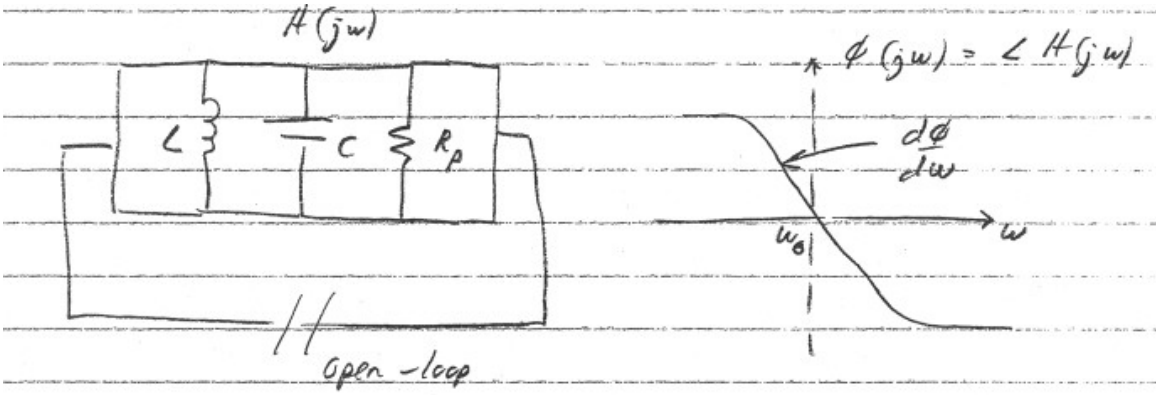


Figure 2.13: LC tank and phase function.

For steady state oscillation, the total phase shift around the feedback loop must be zero.

If the oscillator frequency ω deviates slightly, say due to noise injection, then the larger the change in the loop phase the greater the tendency for the oscillator to return to its center frequency.

The open-loop Q is a measure of how much the closed-loop system opposes variations in the frequency of oscillation.

2.2.2 Dependence of Phase Noise on Q and Offset Frequency

Phase Noise in the Signal Path

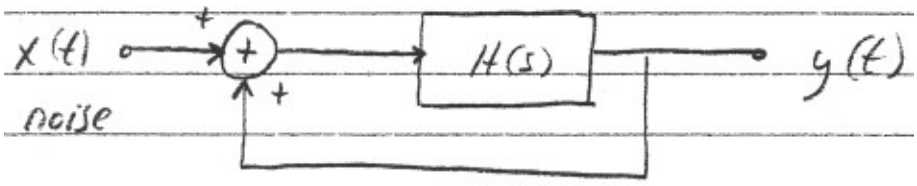


Figure 2.14: Phase noise in the signal path.

$Y(s) = H(s)(X(s) + Y(s))$

$\therefore Y(s)(1 - H(s)) = H(s)X(s)$

$\therefore \frac{Y(s)}{X(s)} = \frac{H(s)}{1-H(s)}$

In the vicinity of the frequency of oscillation $\omega = \omega_o + \Delta\omega, H(j\omega)$ can be approximated by the first two terms if it's Taylor series expansion

$H(j\omega) \approx H(j\omega_o) + \Delta\omega\frac{dH}{d\omega}$

[using $f(x) = f(a) + f'(a)(x - a)$ where $x = \omega, a = \omega_o, x - a = \omega - \omega_o = \Delta\omega$]

$\therefore \frac{Y(j\omega)}{X(j\omega)} = \frac{H(j\omega_o)+\Delta\omega\frac{dH}{d\omega}}{1-(H(j\omega_o)+\Delta\omega\frac{dH}{d\omega})}$

$H(j\omega_o) = +1$ = closed-loop gain of the oscillator = one criterion for oscillation

$\therefore \frac{Y}{X}(\omega_o + \Delta\omega) \approx \frac{1+\Delta\omega\frac{dH}{d\omega}}{-\Delta\omega\frac{dH}{d\omega}}$

assuming that $\Delta\omega\frac{dH}{d\omega} \ll 1$ for small $\Delta\omega$ and H not changing very much from unity over a $d\omega$ change in frequency

$\frac{Y}{X}(\omega_o + \Delta\omega) \approx \frac{-1}{\Delta\omega\frac{dH}{d\omega}}$

$\therefore |\frac{Y}{X}(\omega_o + \Delta\omega)|^2 \approx \frac{1}{(\Delta\omega)^2|\frac{dH}{d\omega}|^2}$

= the factor by which noise introduced into the signal path is multiplied when it appears at the output of the oscillator.

$H(j\omega) = |H|e^{j\phi}$ expressed in polar form

$\therefore \frac{dH}{d\omega} = \frac{d|H|}{d\omega}e^{j\phi} + j|H|\frac{d\phi}{d\omega}e^{j\phi}$

and $|\frac{dH}{d\omega}|^2 = |\frac{d|H|}{d\omega}|^2 + |\frac{d\phi}{d\omega}|^2|H|^2$

for an LC oscillator $\frac{d|H|}{d\omega} \ll |\frac{d\phi}{d\omega}||H|^2$

since the Q is relatively high, $|H|$ is close to unity and $d|H|/d\omega$ cannot be large for oscillation to be sustained since $|H|$ must remain close to unity.

$\therefore |\frac{Y}{X}(j\omega)|^2 =$ noise transfer function $\approx \frac{1}{(\Delta\omega)^2|\frac{d\phi}{d\omega}|^2}$

$|\frac{d\phi}{d\omega}|^2 = (\frac{2}{\omega_o})^2 Q^2 = \frac{4}{\omega_o^2} Q^2$

$\therefore$ $\boxed{|\frac{Y}{X}(j\omega)|^2 = \frac{1}{4Q^2}(\frac{\omega_o}{\Delta\omega})^2}$ Known as "Leeson's Equation"

Noise Shaping in Oscillators

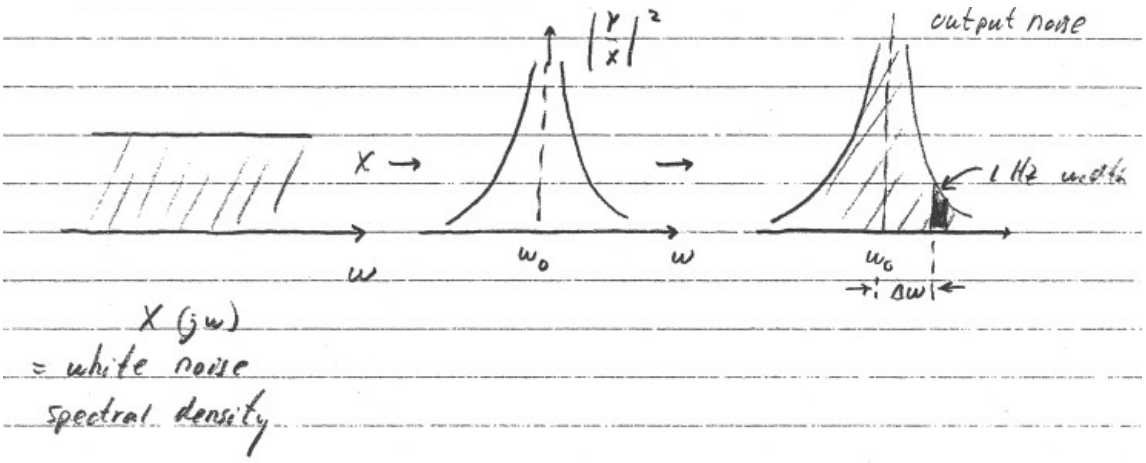


Figure 2.15: Noise shaping in an oscillator.

Therefore, the phase noise of an oscillator is proportional to $1/Q^2$ and $1/(\Delta\omega)^2$.

Other Phase Noise Factors

A physical principle known as the "equipartition theorem" states that the energy of an oscillator tends to distribute itself equally between the different modes of the oscillator.

$\therefore$ the phase noise is typically $\underline{\underline{1/2}}$ of that given above since the Leeson's equation accounts for both amplitude and phase noise.

Phase Noise Also Depends On

a) magnitude of noise source $X(j\omega)$

b) amplitude of power in oscillator itself that is the useful noiseless power of the oscillator

c) nonlinearities resulting in "noise folding" where noise at higher frequencies are down-converted through self-mixing mechanisms to the oscillation frequency

$$\therefore \begin{bmatrix} phase\_noise \\ spectral\_density \end{bmatrix} \alpha \left[(\tfrac{\omega_o}{\Delta\omega})^2 \tfrac{1}{Q^2} \right] \left[nonlinear\_noise\_folding \right] \left[\tfrac{oscillator\_component\_noise\_power}{signal\_power} \right]$$

Noise from nonlinear mixing arises when odd-order nonlinearity in the amplitude leads to intermodulation between and injected noise component at a frequency ω_n and the oscillator carrier creating another component at $2\omega_o - \omega_n$.

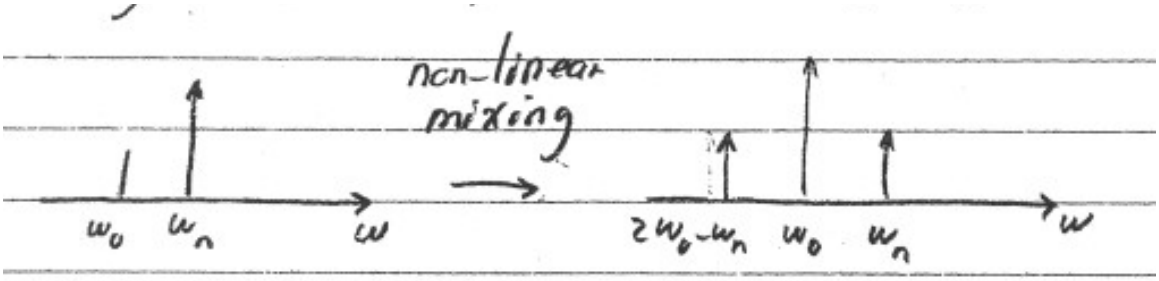


Figure 2.16: Nonlinear mixing.

For an LC tank oscillator, the signal power can be estimated by $I_{bias}^2 R_p$, where R_p is the effective a.c. parallel resistance of the LC tank.

Assuming noise from the active MOSFETs dominates, noise power of the MOSFETs is proportional to g_m of the MOSFETs which is proportional to I_{drain} which is proportional to I_{bias}

$\therefore$ phase noise $\alpha \frac{1}{I_{bias}}$

The larger the inductor of the LC tank, the larger the voltage swing, V_{tank}, since

$V_{tank} \approx I_{bias} R_p = I_{bias} \omega_o L Q$

where $Q = \frac{R_p}{\omega_o L} \therefore R_p = \omega_o L Q$.

Assuming that Q is limited by the losses of the inductor where $Q = \frac{\omega_o L}{R_s}$, $R_s =$ series resistance of the inductor, ar larger inductor will simply increase R_s making Q approximately constant.

$\therefore V_{tank}$ increases as L increases for constant Q and ω_o

Larger $V_{tank} \implies$ larger nonlinearities associated with nonlinear voltage dependent components such as varactors and active transistors $\implies$ more noise folding or more mixing.

$\therefore$ For Minimum Phase Noise

1) make Q as high as possible

2) make I_{bias} as large as is allowed or design for power dissipation specifications

3) use minimum g_m of MOSFETs to satisfy startup condition, $g_m \geq (\alpha_{min}) \frac{RC}{L}$, where α_{min} is a safety factor (usually 2 or 3).

4) use minimum L such that startup condition is still satisfied and such that minimum V_{tank} value is attained according to specifications.

2.3 MOS Varactors

in accumulation: $C_{MOS} = C_{ox} = \frac{\epsilon_o}{t_{ox}} WL = C_{max}$

in depletion: $C_{MOS} = \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}} \approx C_{min}$ where $C_{dep} = \frac{\epsilon_s WL}{W_m}, W_m = \sqrt{\frac{2\epsilon_s(2\phi_F+V_{SB})}{qN_{sub}}}$

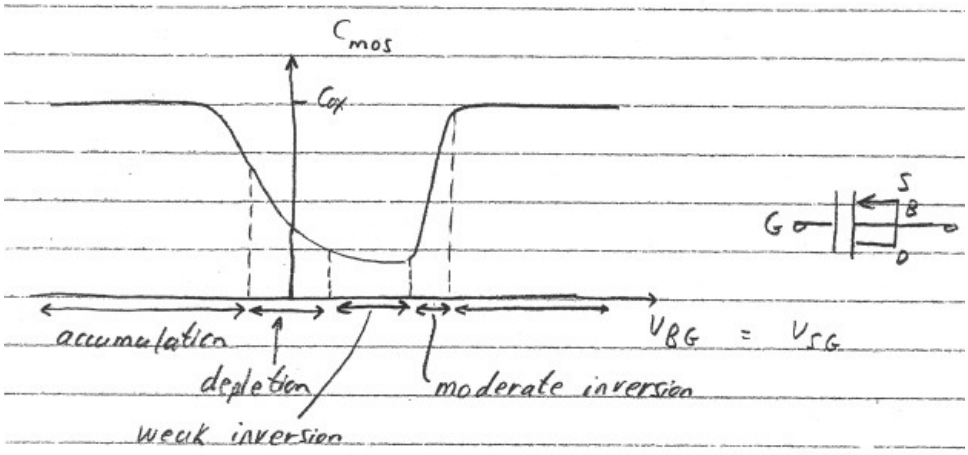


Figure 2.17: Tuning characteristic for PMOS capacitor where Body, Drain and Source are connected together.

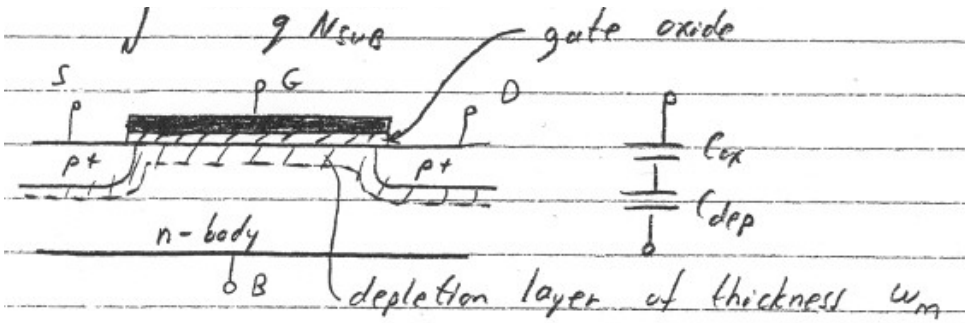


Figure 2.18: MOS internal capacitors.

Practical C_{max}/C_{min} ratios are in the range of 2 taking parasitic device capacitances into account that do not vary strongly with bias.

Designing a PMOS Varactor

1) determine C_{max}/C_{min} ratio required for design:

fractional tuning range = $\frac{f_{max}-f_{min}}{f_o}$

where f_o = center oscillator frequency = $\frac{f_{max}+f_{min}}{2}$

$f_{max} \approx \frac{1}{2\pi\sqrt{L_{tank}C_{min}}}$; $f_{min} \approx \frac{1}{2\pi\sqrt{L_{tank}C_{max}}}$

$\therefore$ $\boxed{\frac{C_{max}}{C_{min}} = \frac{f_{max}^2}{f_{min}^2}}$

2) MOS varactor layout considerations

a) use channel length L_{min} = minimum available L for maximum varactor quality factor Q

b) determine MOS gate total width, W, using

$C_{max} = \frac{\epsilon_o}{t_{ox}} WL \implies W = \frac{t_{os}}{L\epsilon_{ox}}$

c) layout varactor using multi-finger gate to reduce gate series resistance such that Q of varactor is reasonably high.

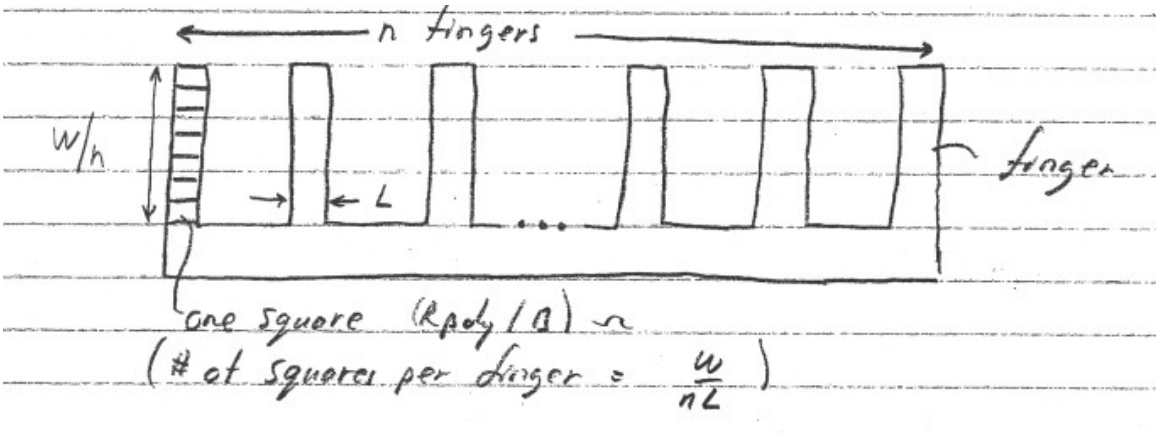


Figure 2.19: Fingered MOSFET gate.

$Q_{min} = \frac{1}{\omega_o C_{max} R_g}$

where R_g = total gate a.c. series resistance = $(R_{poly}/\square)\frac{W}{L}\frac{1}{n^2}$, assuming that the gate contact is composed of polysilicon with sheet resistance $R_{poly}/\square$, and $n = \#$ of fingers and assuming gate is connected from one end.

If the gate is contacted from both ends then divide above formula by 2.

For balanced differential structures, layout two varactors for best matching.

For LC tank oscillators, a high Q for the varactor would be where $Q_{var} \gg Q_{inductor}$, e.g. $Q_{var} = 40$ to 50 when $Q_{inductor} = 10$.

An Inversion Mode MOS (IMOS) Capacitor

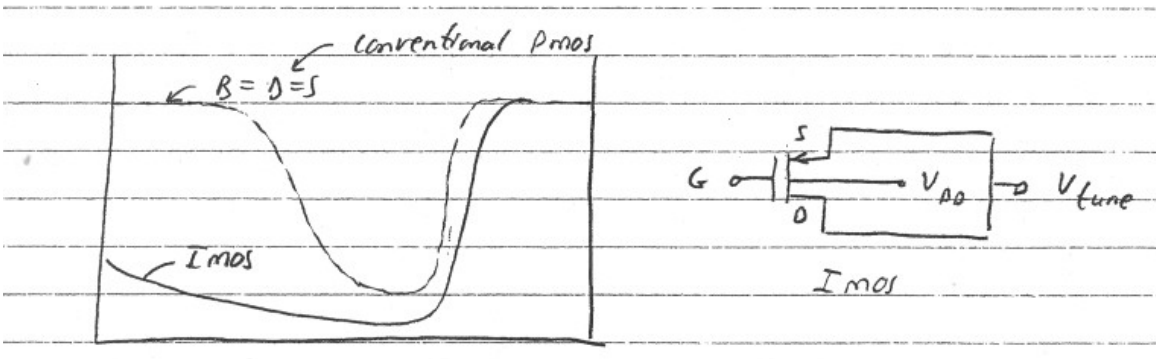


Figure 2.20: IMOS C-V characteristic.

If the Body contact (B) of a PMOS varactor is tied to the most positive voltage (e.g. V_{DD}), then the PMOS varactor will be prevented from entering the accumulation mode.

An inversion mode MOS capacitor is more monotonic with respect to dependence of C_{MOS} on applied tuning voltage.

For large signals, which exist during operation of a VCO, the effective capacitance of the MOS varactor that determines the VCO frequency is actually an average of the instantaneous C_{MOS} over the signal swing.

$\Longrightarrow$ An IMOS varactor will have a larger effective tuning range compared to the conventional PMOS varactor where the Body , Source and Drain are tied together.

2.4 MOSFET Models

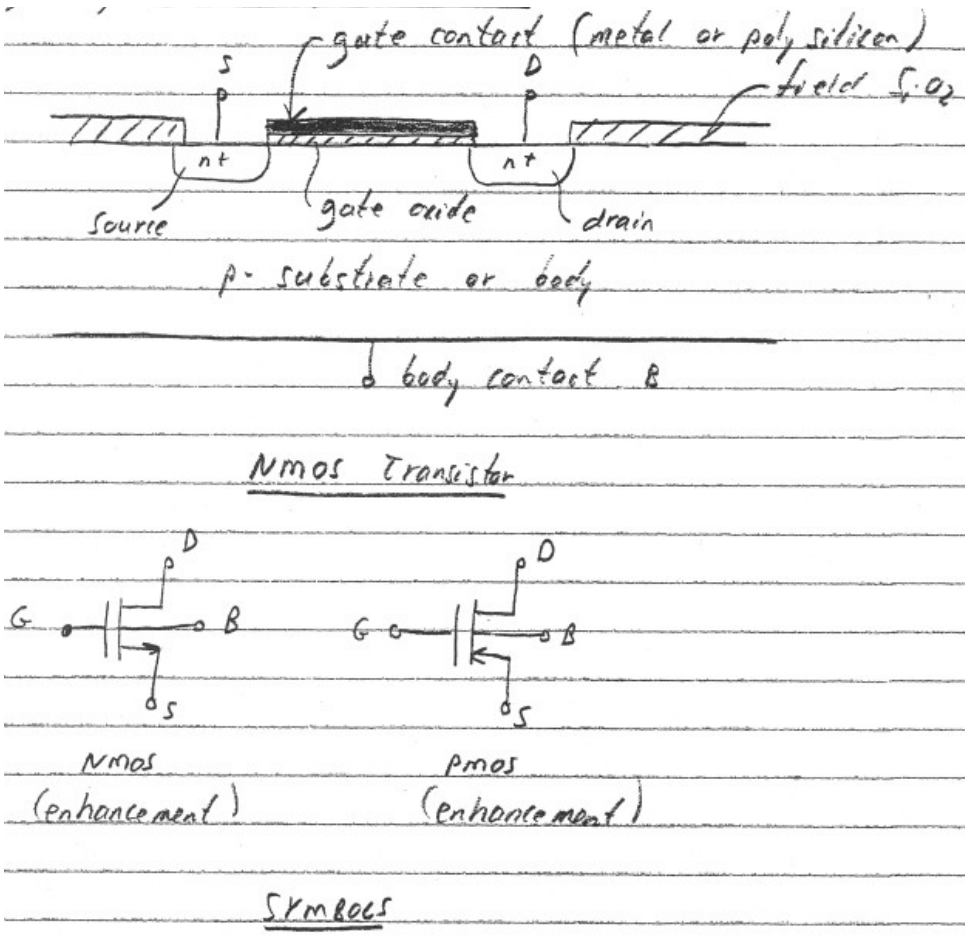


Figure 2.21: MOSFET transistor cross section and symbols.

Large Signal Model for MOSFET

V_t = threshold voltage = $\phi_{ms} + 2\phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}$

where ϕ_{ms} is the work function difference between gate and body, ϕ_f represents the strong inversion condition, Q_b is the bulk depletion charge and Q_{ss} is the interface charge due to defects in gate oxide and at oxide-channel interface.

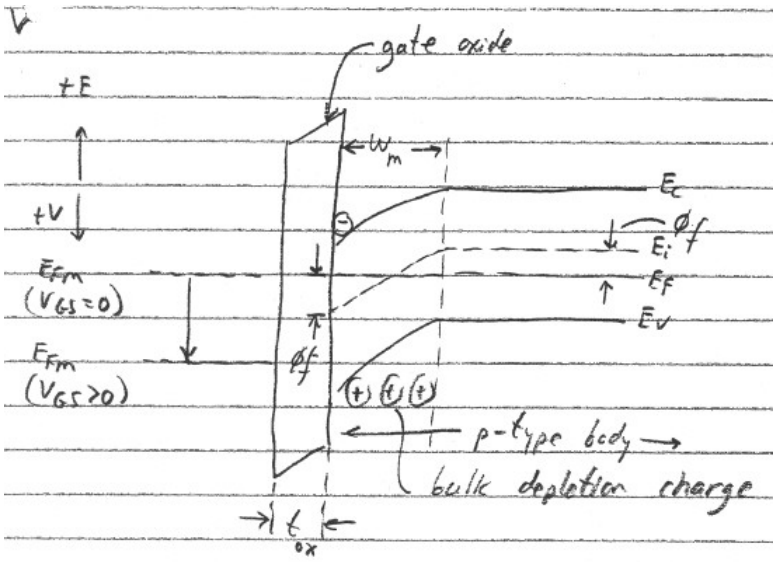


Figure 2.22: MOSFET energy band diagram.

$$\boxed{V_t = V_{to} + \gamma(\sqrt[2]{2\phi_f + V_{SB}} - \sqrt[2]{2\phi_f})}$$

where V_{to} is the threshold voltage for $V_{SB} = 0$, γ is the "gamma" factor, and V_{SB} is the source to body bias "body effect".

$$Q_b = \sqrt[2]{2q\epsilon_s N_A(2\phi_f + V_{SB})}$$

$$\gamma = \frac{\sqrt[2]{2q\epsilon_s N_A}}{C_{ox}}; \phi_f = V_T ln(\frac{N_A}{n_i})$$

N_A = body doping; $\epsilon_s \approx 10^{-12}$ F/cm for Si; n_i =intrinsic carrier concentration $\approx 1.5 \times 10^{10} cm^{-3}$; C_{ox} = Gate oxide capacitance per unit Gate width, W, = $\frac{\epsilon_{ox}}{t_{ox}}$; ϵ_{ox} = permittivity of oxide (SiO_2) = $(3.9)(8.85 \times 10^{-14})$ F/cm= $\epsilon_r \epsilon_o$; t_{ox} = Gate oxide thickness (typically 100s of Å).

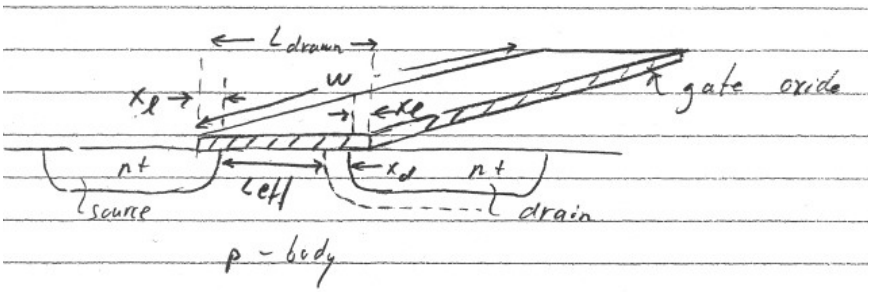


Figure 2.23: 3D MOSFET.

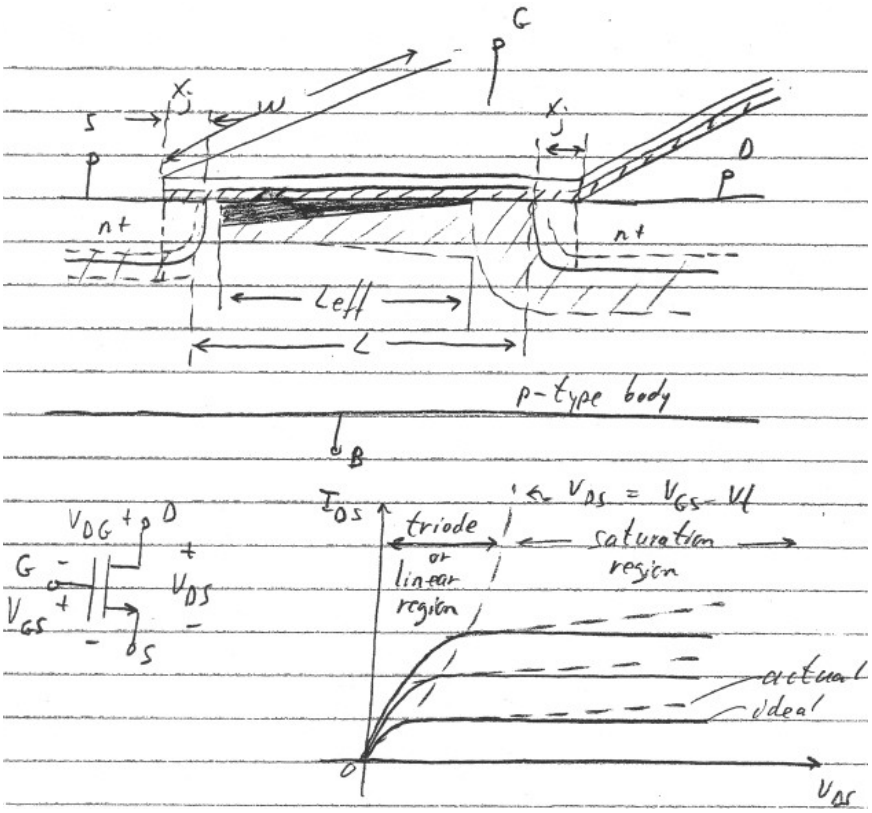


Figure 2.24: Detailed 3D MOSFET, and MOSFET output Drain characteristics.

$L_{eff} = L_{drawn} - 2X_l - X_d$

X_l = lateral diffusion of Source and Drain under Gate

X_d = space-charge-layer width of Body-Drain reverse-biased diode under Gate.

$\boxed{I_{DS} = \frac{k'W}{2L_{eff}}[2(V_{GS} - V_t)V_{DS} - V_{DS}^2]}$ $\leftarrow$ linear region ($V_{DS} < V_{GS} - V_t$)

where $k' = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$, μ_n = channel mobility.

When channel potential at drain end of inversion channel under Gate reaches $V_{GS} - V_t$ due to V_{DS}, the channel becomes pinched-off at this point onwards towards the Drain.

Hence, for $V_{DS} \geq V_{GS} - V_t$, pinch-off occurs and ideally the Drain current I_{DS} becomes independent of V_{DS} such that:

$I_{DS} = \frac{k'W}{2L_{eff}}(V_{GS} - V_t)^2$ for $V_{DS} \geq V_{GS} - V_t$.

As V_{DS} increases beyond $V_{GS} - V_t$, the pinch-off point of the channel moves towards the Source shortening the channel length L_{eff} causing an increase in I_{DS}

To model this: $\boxed{I_{DS} = \frac{k'W}{2L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})}$ for $V_{DS} \geq V_{GS} - V_t$

where $\lambda = \frac{1}{V_A}$; V_A = Early voltage.

Small Signal for MOSFET in Saturation

Recall:

$V_t = V_{to} + \gamma(\sqrt[2]{2\phi_f + V_{SB}} - \sqrt[2]{2\phi_f})$

$\gamma = \frac{\sqrt[2]{2q\epsilon_s N_A}}{C_{ox}}$

$I_{DS} = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$ in saturation

$k' = \mu_n C_{ox}$

$V_A = \frac{1}{\lambda} = \frac{I_D}{\partial I_D / \partial V_{DS}}$

I_{DS} is a function of both V_{GS} and V_{BS} (since I_{DS} is a function of V_t and V_t is a function of V_{BS}).

Note: $V_{BS} = -V_{SB}$.

$\therefore$ The small signal model will possess two transconductance generators.

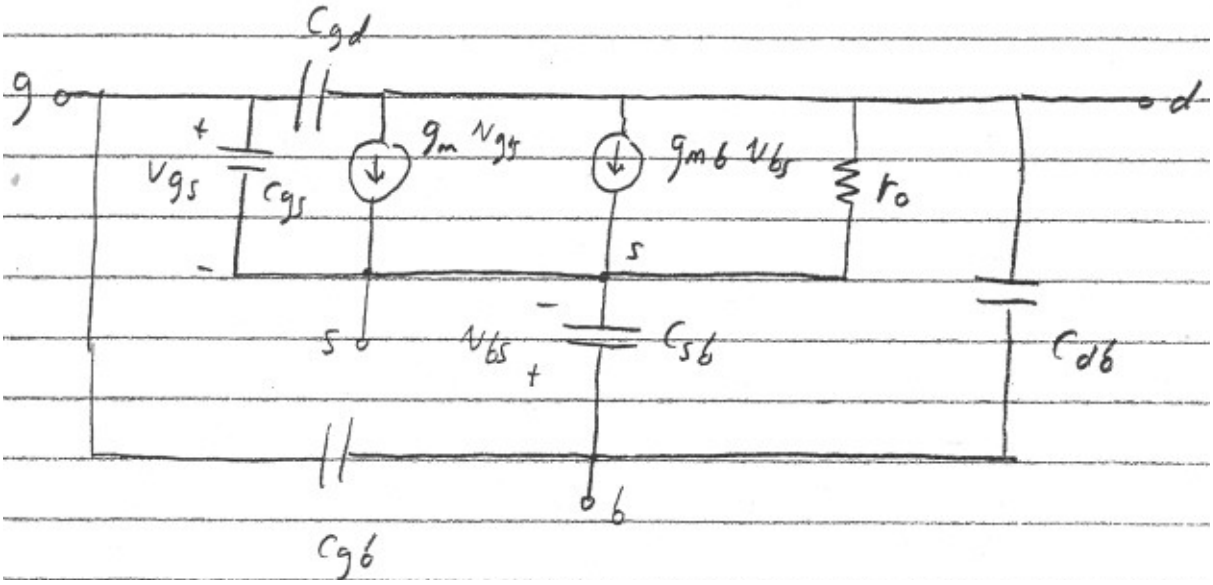


Figure 2.25: MOSFET small signal equivalent circuit.

$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{k'W}{L}(V_{GS} - V_t)(1 + \lambda V_{DS}) \approx \frac{k'W}{L}(V_{GS} - V_t) = \sqrt[2]{2k'\frac{W}{L}I_{DS}}$ if $\lambda V_{DS} \ll 1$

$g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} = -\frac{k'W}{L}(V_{GS} - V_t)(1 + \lambda V_{DS})\frac{\partial V_t}{\partial V_{BS}}$

$V_t = V_{to} + \gamma(\sqrt[2]{2\phi_f - V_{BS}} - \sqrt[2]{2\phi_f})$

$\frac{\partial V_t}{\partial V_{BS}} - \frac{\gamma}{2}\sqrt[2]{2\phi_f - V_{BS}} = \frac{-\gamma}{2\sqrt[2]{2\phi_f + V_{SB}}} = -\chi$

$W_m = \sqrt[2]{\frac{2\epsilon_s(2\phi_f + V_{SB})}{qN_A}}$

$\gamma = \frac{\sqrt[2]{2q\epsilon_s N_A}}{C_{ox}}$

$C_{dep} = \frac{\epsilon_s}{W_m}$

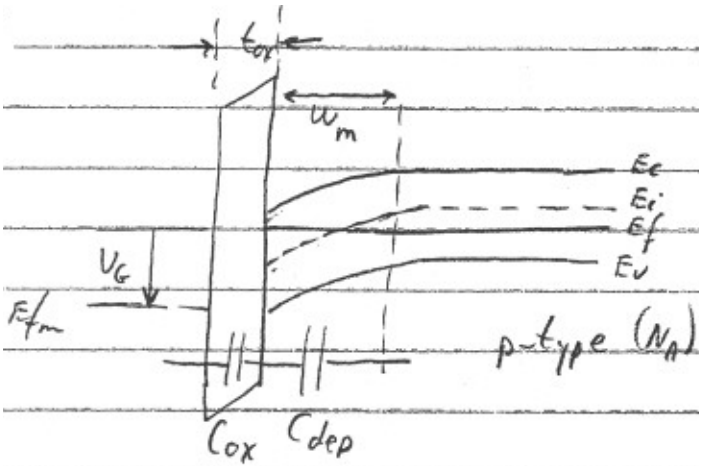


Figure 2.26: NMOS depletion capacitance.

$\therefore \chi = \frac{\gamma}{2\sqrt[2]{2\phi_f + V_{SB}}} = \frac{\sqrt[2]{2q\epsilon_s N_A}}{C_{ox}} = \frac{1}{2}\sqrt[2]{\frac{2\epsilon_s}{qN_A}}\frac{1}{W_m} = \frac{\epsilon_s}{W_m}\frac{1}{C_{ox}} = \frac{C_{dep}}{C_{ox}}$

$\therefore \chi = \frac{C_{dep}}{C_{ox}}$ or $\frac{\partial V_t}{\partial V_{BS}} = -\frac{C_{dep}}{C_{ox}} = -\chi$

where C_{dep} = depletion layer capacitance below Gate oxide in channel region.

$\therefore g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} = -\frac{k'W}{L}(V_{GS} - V_t)(1 + \lambda V_{DS})\frac{\partial V_t}{\partial V_{BS}} = \frac{k'W}{L}(V_{GS} - V_t)(1 + \lambda V_{DS})\frac{\gamma}{2\sqrt[2]{2\phi_f + V_{SB}}} = \frac{\gamma k'(W/L)(V_{GS} - V_t)(1 + \lambda V_{DS})}{2\sqrt[2]{2\phi_f + V_{SB}}} = \frac{\gamma\sqrt[2]{k'(W/L)I_{DS}}}{\sqrt[2]{2(2\phi_f + V_{SB})}}$ assuming $\lambda V_{DS} \ll 1$.

Using $g_m = \frac{k'W}{L}(V_{GS} - V_t)(1 + \lambda V_{DS})$,

$\frac{g_{mb}}{g_m} = \frac{-\frac{k'W}{L}(V_{GS}-V_t)(1+\lambda V_{DS})\frac{\partial V_t}{\partial V_{BS}}}{\frac{k'W}{L}(V_{GS}-V_t)(1+\lambda V_{DS})} = -\frac{\partial V_t}{\partial V_{BS}}$

$\therefore \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt[2]{2\phi_f+V_{SB}}} = \chi = \frac{C_{dep}}{C_{ox}}$

(χ usually ranges from 0.1 to 0.3)

Note: g_{mb} arises from the Body being held at a constant voltage and a small signal being applied to the Source.

$r_o = (\frac{\partial I_D}{\partial V_{DS}})^{-1} = (\lambda\frac{k'}{2}\frac{W}{L}(V_{GS}-V_t)^2)^{-1} = (\lambda I_{DS})^{-1} = \frac{1}{\lambda I_{DS}} \equiv \frac{V_A}{I_D}$ where $V_A = \frac{1}{\lambda}$ = a.c. output resistance

C_{gs} = the only "intrinsic" capacitance while all others are considered parasitic.

C_{sb} = the parasitic depletion-region capacitance between the substrate and Source.

C_{db} = the parasitic depletion-region capacitance between the substrate and Drain.

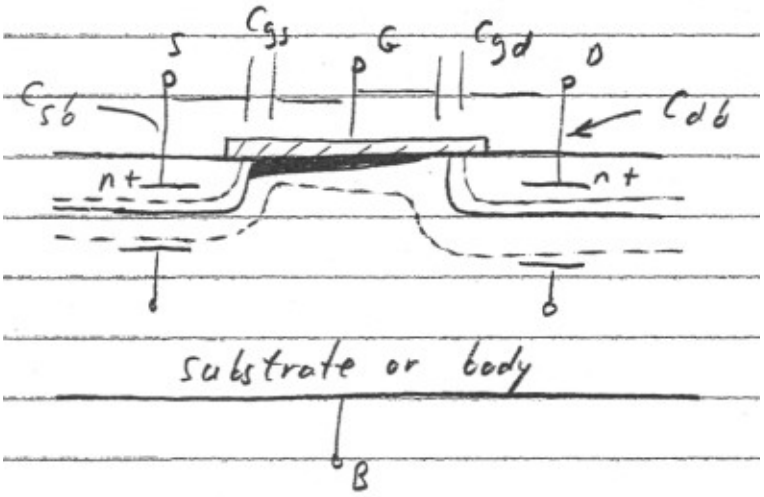


Figure 2.27: NMOS capacitances.

$C_{sb}\frac{C_{sbo}}{\sqrt[2]{1+\frac{V_{SB}}{\psi_o}}} =; C_{db} = \frac{C_{dbo}}{\sqrt[2]{1+\frac{V_{DB}}{\psi_o}}}$

C_{gb} = capacitance between Gate and substrate that models parasitic oxide capacitance between Gate contact materials and substrate outside the active device area.

- is a constant capacitance
- models coupling between polysilicon, metal interconnects and substrate

C_{gs} and C_{gd} Capacitances

In ohmic region of device operation:

$C_{gs} = C_{gd} = \frac{1}{2} C_{ox} W L$

In saturation region of device operation:

i) C_{gd} consists of a constant parasitic oxide-capacitance due to Gate overlap of the Drain region.

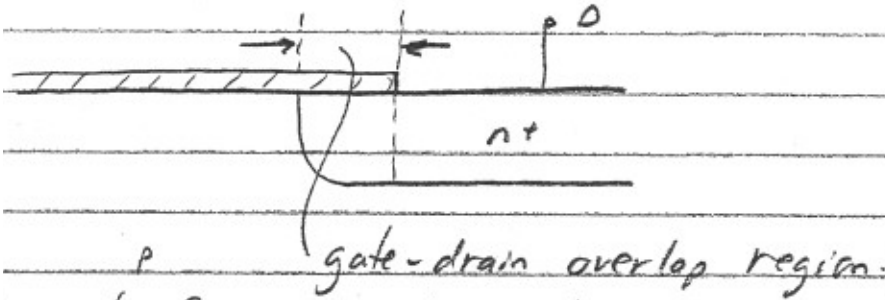


Figure 2.28: Gate-Drain overlap region.

- intrinsic portion of $C_{gd} \approx 0$ in saturation since V_D (Drain voltage) has little influence on channel charge beneath Gate.

ii) $C_{gs} = \frac{2}{3} C_{ox} W L$

Transition Frequency, f_T

Assuming that the input capacitance is dominated by C_{gs} one can write $f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs}}$

by comparison to the formula for a bipolar transistor.

Substituting for g_m and C_{gs} (using $g_m = k'\frac{W}{L}(V_{GS} - V_t) = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)$ and $C_{gs} = \frac{2}{3}C_{ox}WL$):

$$\begin{aligned} f_T(MOSFET) &= \frac{1}{2\pi}\frac{g_m}{C_{gs}} \\ &= \frac{\mu_n C_{ox}}{2\pi}\frac{W}{L}(V_{GS} - V_t)\frac{1}{C_{gs}} \\ &= \frac{\mu_n C_{ox}}{2\pi}\frac{W}{L}(V_{GS} - V_t)[\frac{3}{2}\frac{1}{C_{ox}WL}] \\ &= \frac{3}{2}\frac{\mu_n}{2\pi L^2}(V_{GS} - V_t) \end{aligned}$$

$$\begin{aligned} f_{Tmax}(BIPOLAR) &= \frac{1}{2\pi\tau_F} \\ &= \frac{1}{2\pi\frac{W_B^2}{2D_n}} \\ &= 2\frac{1}{2\pi}\frac{\mu_n}{W_B^2}V_T \end{aligned}$$

where $D_n = V_T\mu_n$.

Comparing:

$$\begin{aligned} f_T(MOSFET) &= \frac{3}{2}\frac{\mu_n}{2\pi L^2}(V_{GS} - V_t) \\ f_T(BJT) &= 2\frac{\mu_n}{2\pi W_B^2}V_T \end{aligned}$$

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